COBEP–SPEC 2015 Tutorial

Digital Control in Power Electronics

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Tutorial Outline

- Introduction on Digital Control in Power Electronics
- Part I – Digital control basics
- Part II – Modulation delay, basic modeling techniques and controller design
- Part III – Quantization effects
- Part IV – Advances in Digital Control in High-Frequency dc-dc Converters
- Part V – Oversampled Current Controller for Grid-Connected Inverter

Introduction: Digital Control in Power Electronics

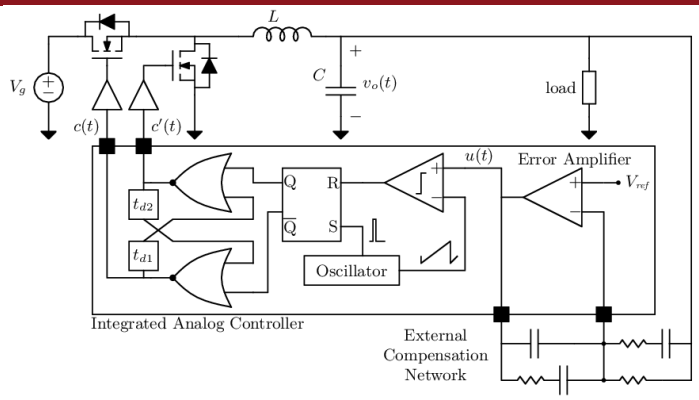
- Digital control *using microcontrollers or DSP chips* has long been used in power electronics at relatively high power levels and at relatively low switching frequencies, as in:
  - Grid-connected three-phase inverters and rectifiers
  - Motor drives
  - Uninterruptible power supplies

$P \gtrsim$ several kW
$f_s \lesssim$ tens of kHz
Traditionally
micro- or DSP-controlled

- Major advances in practical digital control for *high-frequency* switched-mode power supplies (SMPS) have also been introduced in application areas such as:
  - Mobile and desktop electronics
  - Server power distribution systems
  - Telecom/datacom power management
  - Energy-efficient lighting
  - Distributed PV optimizers

$P \lesssim$ hundreds of W
$f_s \gtrsim$ hundreds of kHz
Traditionally
analog-controlled!

Traditional Analog PWM Control: Voltage-Mode Buck Example



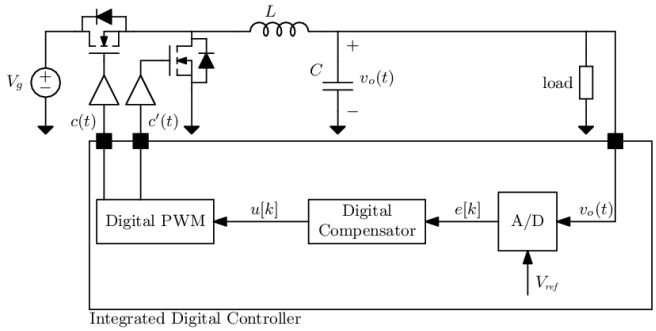
Pros:

- More than 30 years old technology, widely available
- Simple circuitry, well-known design techniques
- Achievable closed-loop bandwidth $f_c \sim f_s/20$–$f_s/5$ depending on the control strategy

Cons:

- No flexibility, system parameters set through passive components
- Sensitivity to process and temperature variations
- System interface and (digital) power management features possible through added complexity of microcontroller with A/D and D/A hooks

Why not Digital Control?

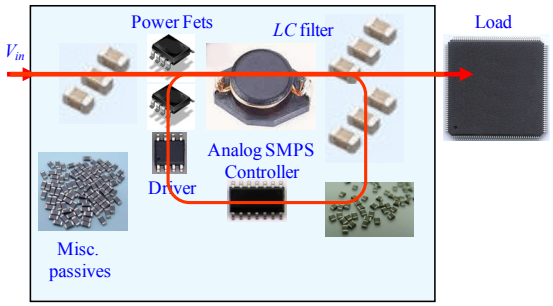


- Scaling, performance and cost advances in digital VLSI are rapid
- External passive components no longer required for loop compensation
- Programmability, flexibility, built-in system interface
- Ability to implement more advanced control techniques

- A/D or DPWM can be more complex and costly than an entire analog PWM controller
- Standard, cost-effective micro-controllers or DSPs are too slow and too complex for majority of mainstream high-frequency SMPS operating in the hundreds of kHz to MHz

Analog vs. "brute force" Digital Loop

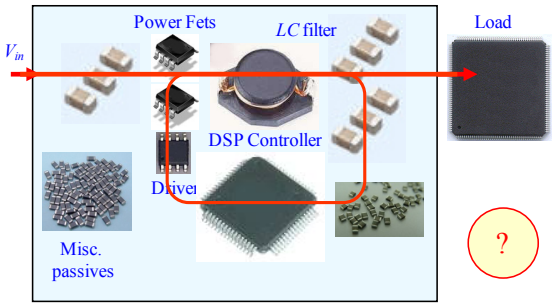
"Analog" dc–dc SMPS



- Switching frequency: 1 MHz
- Loop bandwidth: 100 kHz
- Ma

For high-frequency DC-DC applications, new approaches are needed to exploit the advantages of digital VLSI and signal processing technologies

"Digital" dc–dc SMPS

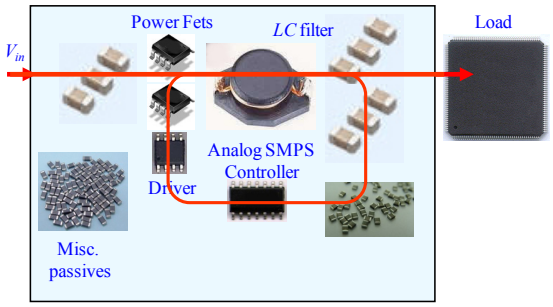


- DSP-based controller:
  - Fast, high-resolution A/D
  - Very high clock-rate DPWM
  - Slow, software-based compensation
  - Poorly flexibile architecture
- Switching frequency: 50 kHz
- Loop bandwidth: 3 kHz
- High cost, no obvious benefits

[65] D. Maksimovic and P. Mattavelli, "Digital Control in Power Electronics: A Power Supply Perspective," in *Proc. 15th International Power Electronics and Motion Control Conference and Exposition* (EPE-PEMC ECCE Europe), Sep. 2012

Analog vs. Hardware-Optimized Digital Loop

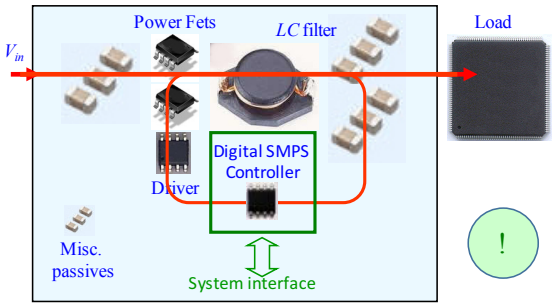
"Analog" dc–dc SMPS



- Switching frequency: 1 MHz
- Loop bandwidth: 100 kHz
- Mat…

Potentials for significant improvements in both performance and system intergration

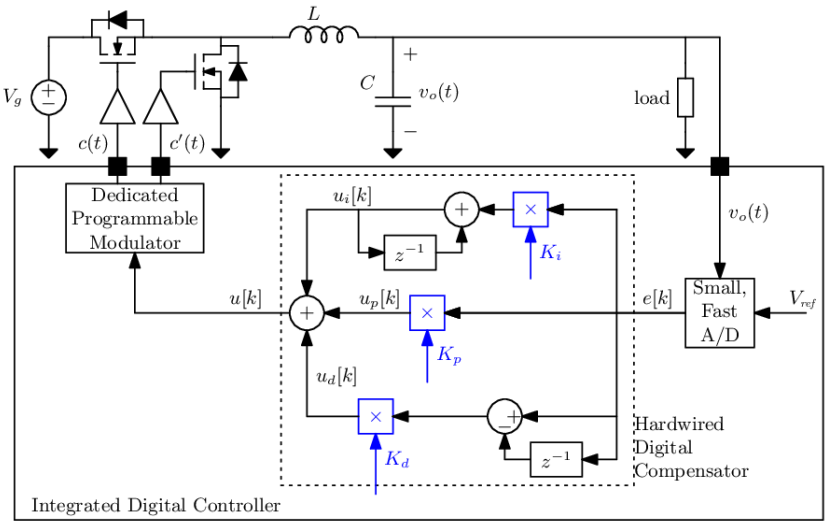
"Digital" dc–dc SMPS



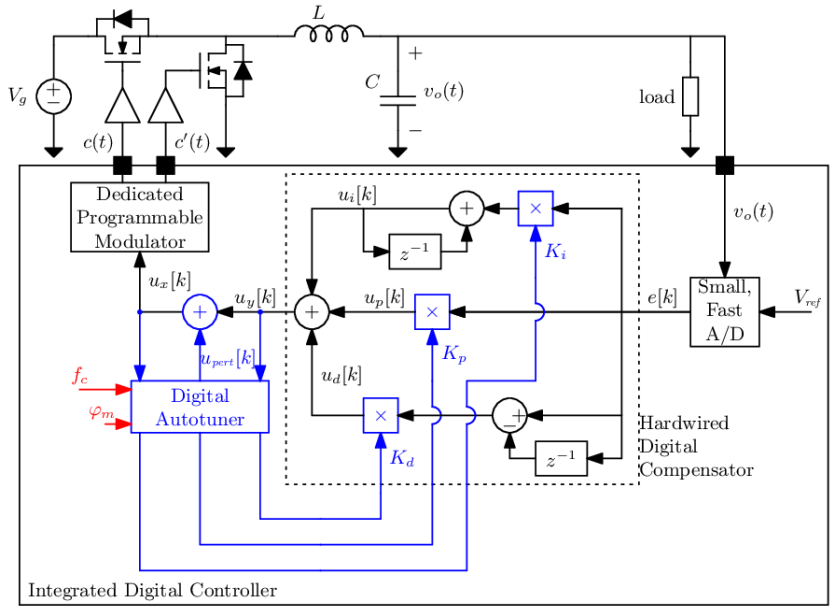
- Custom-designed digital IC:
  - Small-area, low-cost digital CMOS
  - Optimized A/D and DPWM
  - Fast, programmable hardwired compensator
  - Scalable, HDL-based design
  - Fewer discrete components
- Switching frequency: 1 MHz
- Loop bandwidth: 100 kHz
- Lower cost

[65] D. Maksimovic and P. Mattavelli, "Digital Control in Power Electronics: A Power Supply Perspective," in *Proc. 15th International Power Electronics and Motion Control Conference and Exposition* (EPE-PEMC ECCE Europe), Sep. 2012

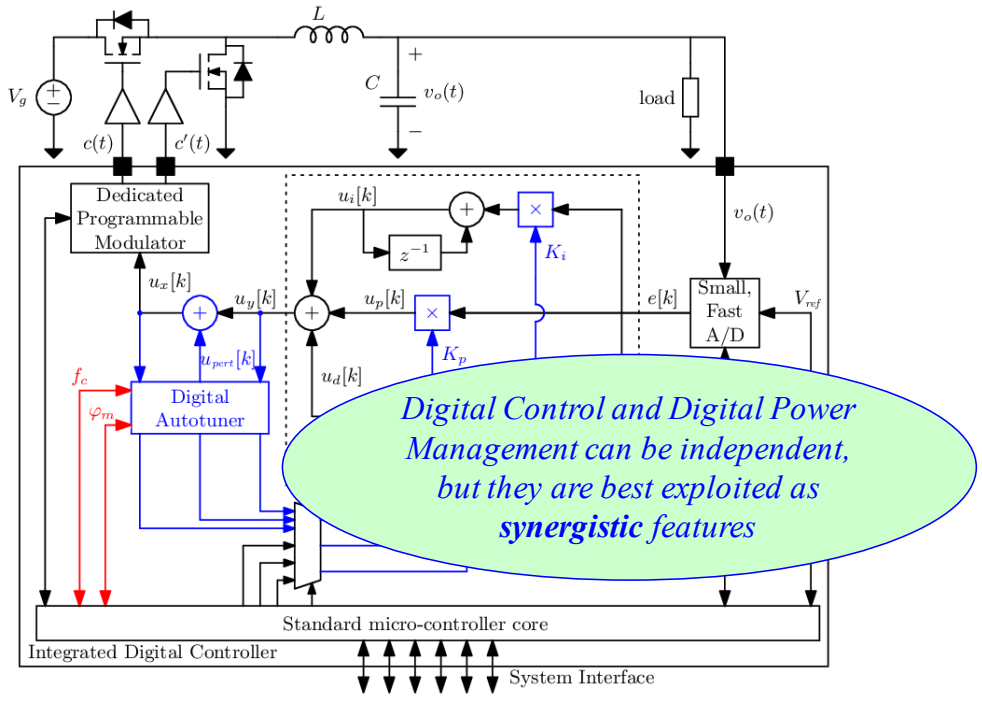
Digitally-Controlled Point-of-Load Converter



More Features: Digital Autotuning



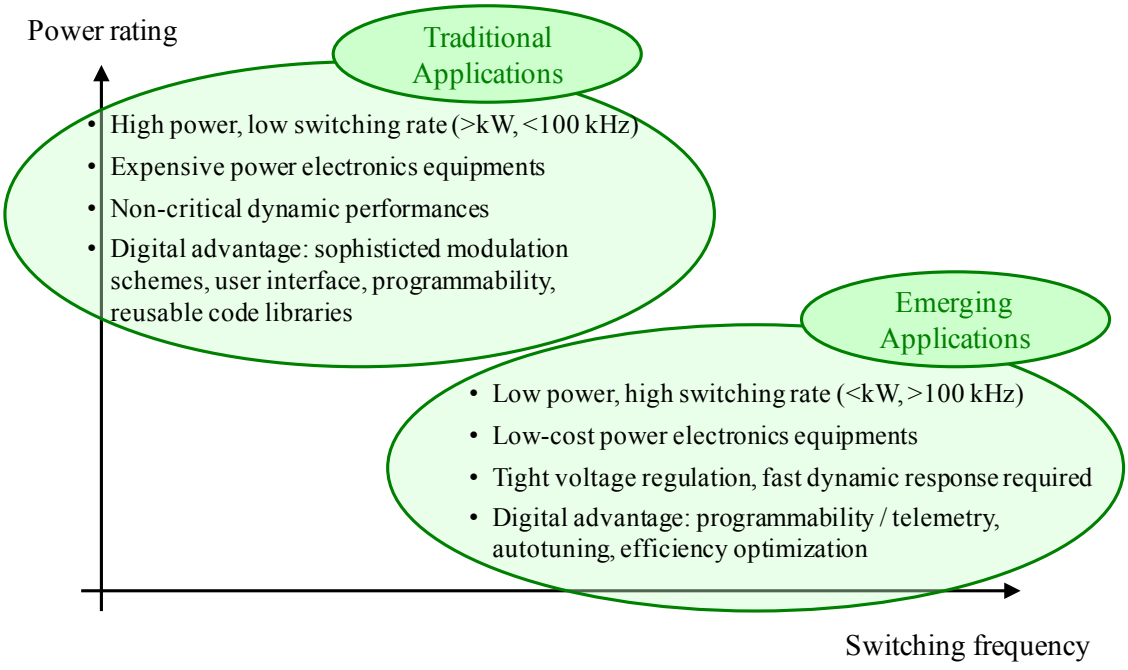
From Digital Control to Digital Power Management



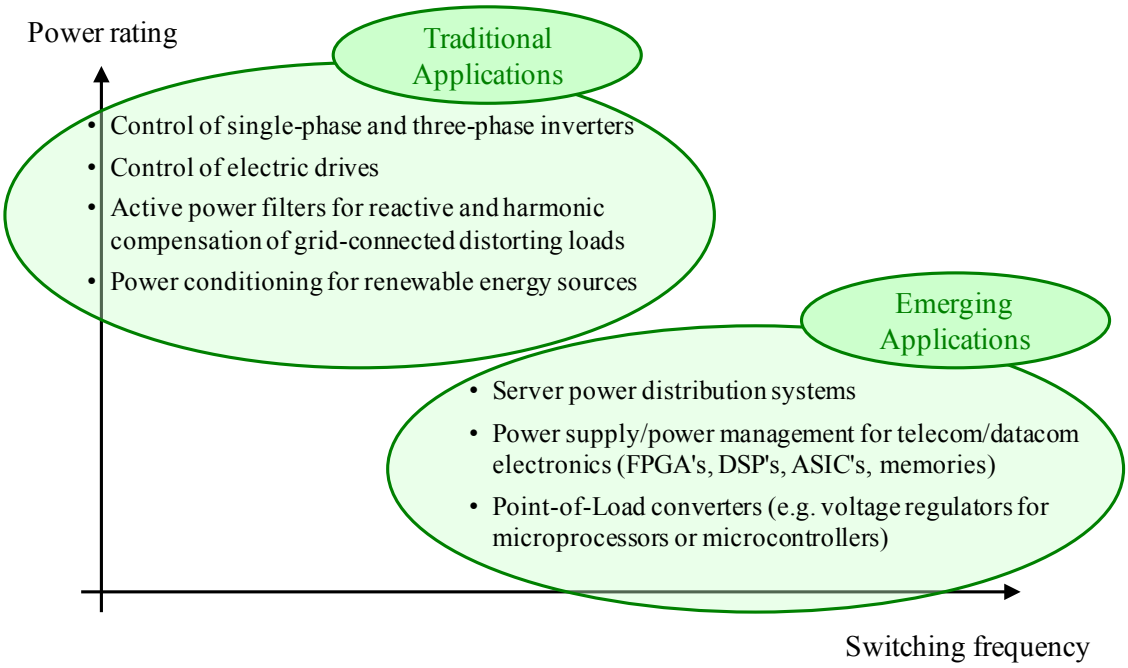
Digital Control in Power Electronics

- Pros:
  - Rubustness against disturbances and noise
  - Stability of control characteristics over time and temperature
  - Field programmability: control parameters, and sometimes the control law itself, can be re-programmed without hardware modifications
  - Interface and communication: the digital controller can interact with other units or with a user interface via suitable communication protocols (e.g. CAN, I^2C etc…)
- Cons:
  - Cost of the control platform as opposed to analog solutions, when these exist (although price of digital IC's has been steadily decreasing over the last few years)
  - Performances: analog solutions, when they exist, easily offer better performances in terms of regulation and dynamic response
  - Less "standard" design for the traditional analog designer, as it involves sampled-data systems analysis

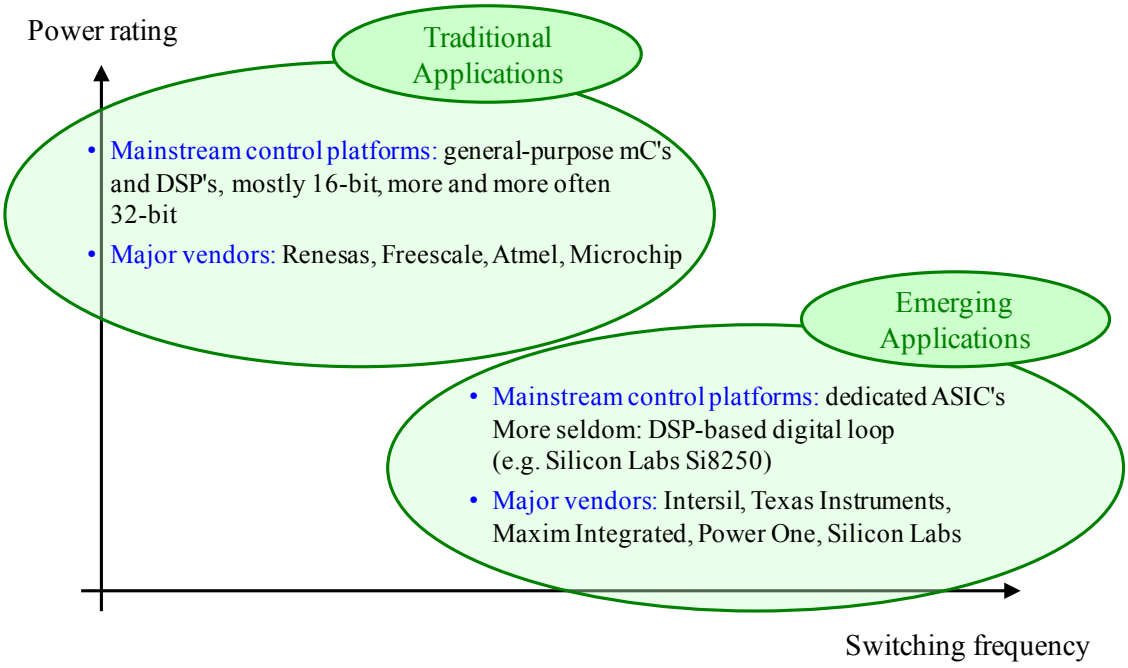
Traditional and Emerging Applications



Traditional and Emerging Applications



Traditional and Emerging Applications

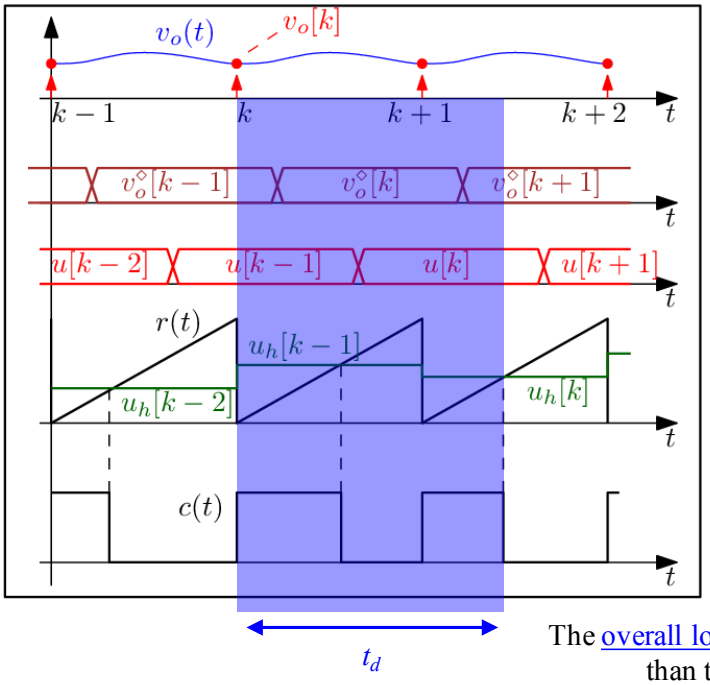


Main Digital Platforms

- Microcontrollers and DSP's
- Application-Specific Integrated Circuits (ASIC)
- Field-Programmable Gate Arrays (FPGA)

- Control algorithm is software-implemented and executed by a CPU
- High computational resources and dedicated I/O
- Typically equipped with A/D and D/A converters, and with medium- to high-resolution PWM modulators.
- Controller implementation is relatively fast and not critical

Typical Timing Diagram of a Microcontroller-Based Digital Loop

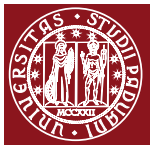


Interrupt and A/D conversion

Execution of control algorithm and wait for the DPWM to latch $u[k]$

Digital PWM Modulation

The overall loop delay t_d is typically longer than the switching cycle T_s



Main Digital Platforms

- Microcontrollers and DSP's
- Application-Specific Integrated Circuits (ASIC)
- Field-Programmable Gate Arrays (FPGA)

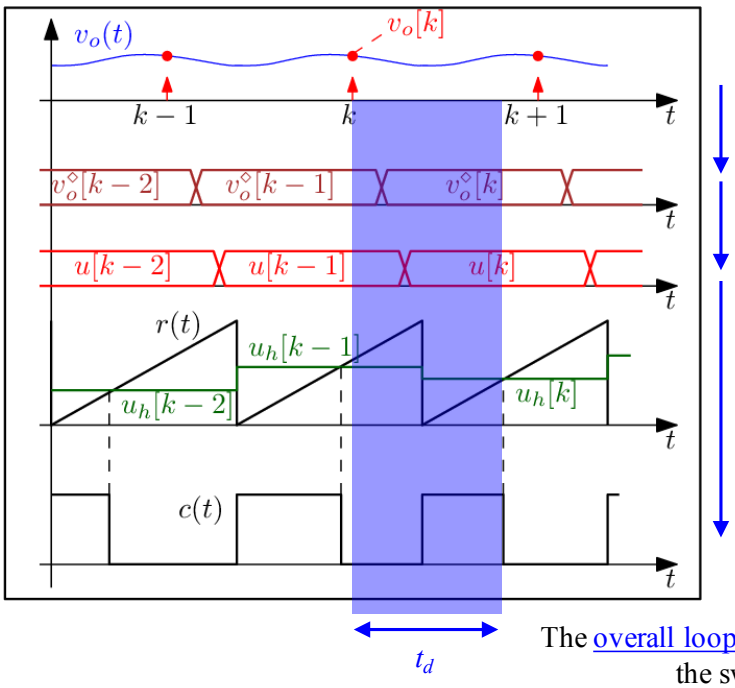
- Hardware-based controller realized on a dedicated integrated circuit ➔ Full-custom design
- Design flexibility enables low-cost, *ad hoc* solutions
- Speed: computational delays typical of μC/DSP platform are largely reduced ➔ Fast controllers optimized for critical applications
- Disadvantage of a long *time to market*

Main Digital Platforms

- Microcontrollers and DSP's
- Application-Specific Integrated Circuits (ASIC)
- Field-Programmable Gate Arrays (FPGA)

- General-purpose digital IC's consisting of a set of logic resources which can be interconnected in a user-programmable way
- Field programmability
- Reduced *time to market* with respect to full-custom designs
- Controller is hardware-based ➔ advantages comparable to ASIC implementations in terms of flexibility

Typical Timing Diagram of an ASIC- or FPGA-based Controller



A/D Conversion

Control command calculation

Digital PWM modulation

The overall loop delay t_d can be a fraction of the switching cycle T_s

Example of a Voltage-Mode Control Digital IC

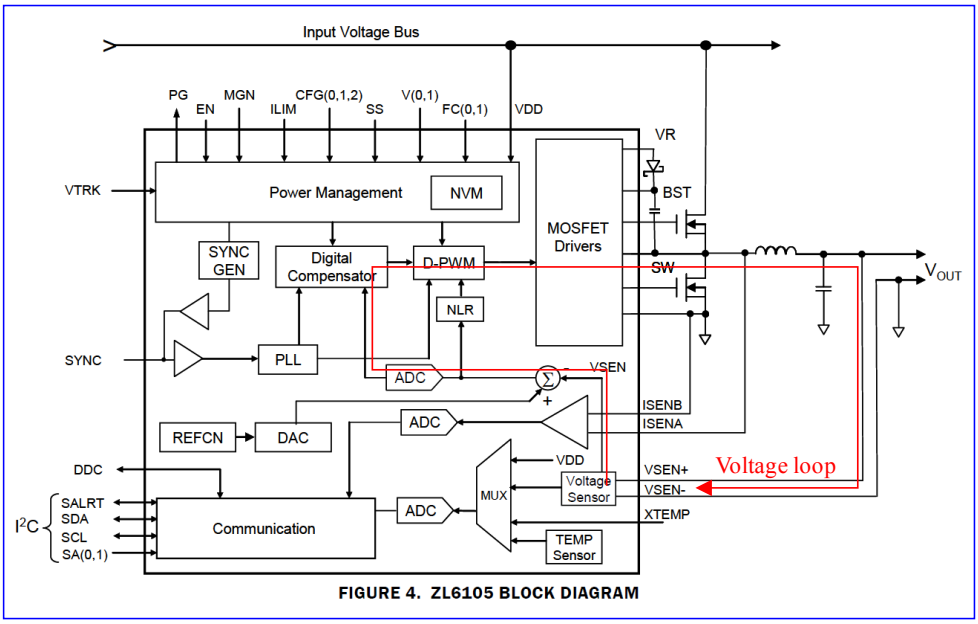


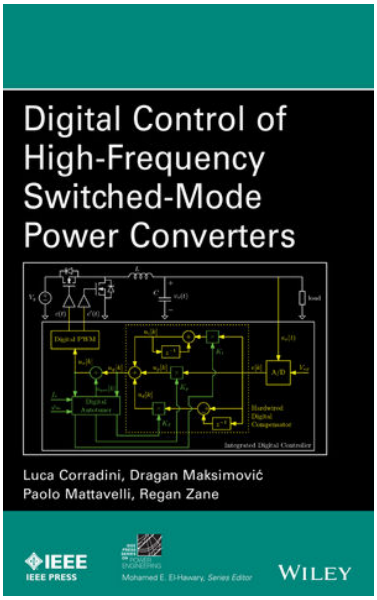
FIGURE 4. ZL6105 BLOCK DIAGRAM

http://www.intersil.com/content/dam/Intersil/documents/fn69/fn6906.pdf

Part I
Digital Control Basics

Textbook on Digital Control in Power Electronics

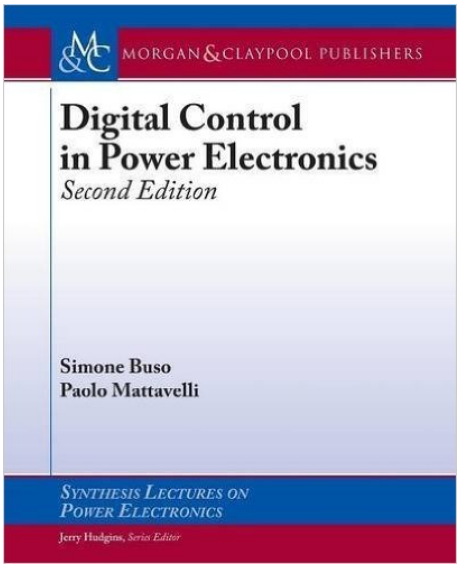
- L. Corradini, D. Maksimović, P. Mattavelli and R. Zane, "Digital Control of High-Frequency Switched-Mode Power onverters," 1st ed. Wiley-IEEE Press, 2015
  - Comprehensive treatment of digital control theory for power converters
  - Enables readers to successfully analyze, model, design, and implement voltage, current, or multiloop digital feedback loops around switched-mode power converters
  - Practical examples are used throughout the book to illustrate applications of the techniques developed:
    - Matlab examples and simulations
    - Verilog and VHDL sample codes



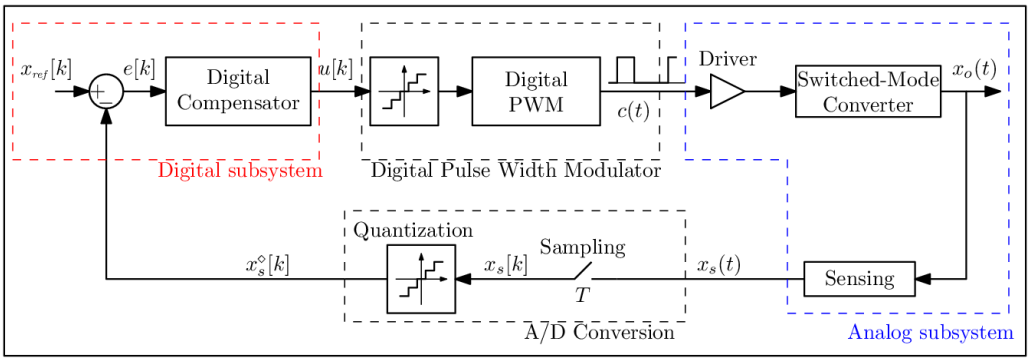
http://eu.wiley.com/WileyCDA/WileyTitle/productCd-1118935101.html

Textbook on Digital Control in Power Electronics

- Introductory knowledge of the digital control techniques applied to power converters
- Different control approached applied to the half-bridge voltage source inverter, considered both in its single- and three-phase implementation.
- Application to inverter output current and voltage control, ending with the relatively more complex VSI applications related to the so called *smart-grid* scenario

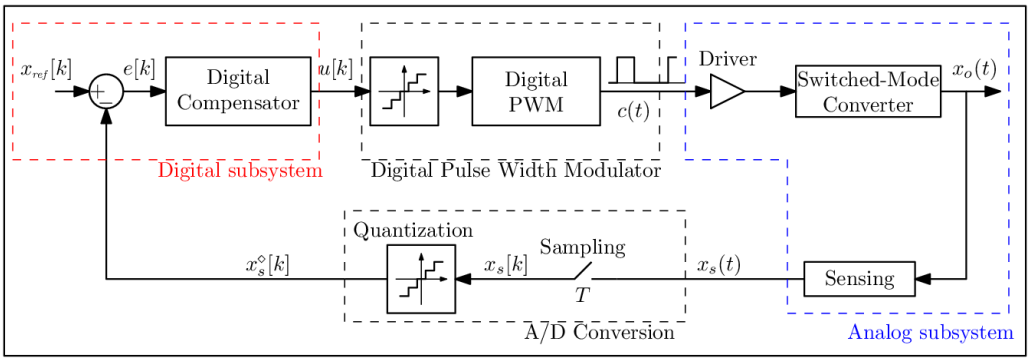


Digital Control of a Switched-Mode Power Converter



- **Sampled data system,** in which both analog and digital subsystems coexist, interfaced by A/D and D/A converters:
  - **Analog subsystems** process continuous-time, continuous-amplitude signals.
  - **Digital subsystems** process discrete-time, quantized-amplitude signals.

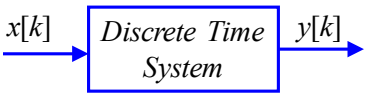
Digital Control of a Switched-Mode Power Converter



- **Typical control objectives:**
  - Regulation of $x_o(t)$ at a reference value against disturbances of various kind.
    Example: output voltage regulation in DC/DC converters.
  - Tracking of a given time-varying profile.
    Example: digital current or voltage control of a DC/AC inverter.

Discrete-Time Systems Basics

A discrete time system processes a discrete time sequence $x[k]$ and outputs a discrete time signal $y[k]$. A sampling period T defines the rate at which the signals x and y are processed and updated.



As long as linear, time invariant systems are considered, the time domain relationship between x and y can always be written as:

$$y[k] = (g * x)[k] = \sum_{n=0}^{+\infty} g[n] \cdot x[k-n]$$

, where $g[k]$ represents the system impulse response.

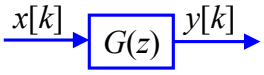
Discrete-Time Systems Basics

The Z-Transform $X(z)$ of a discrete-time sequence $x[k]$ is defined as:

$$X(z) \equiv \sum_{n=0}^{+\infty} x[n] \cdot z^{-n}$$

The Z-Transform plays for discrete time systems a role similar to that of the Laplace Transform for analog systems:

1) The Z-Transform $G(z)$ of the system impulse response $g[k]$ represents the system transfer function



$$Y(z) = G(z) \cdot X(z)$$

Discrete-Time Systems Basics

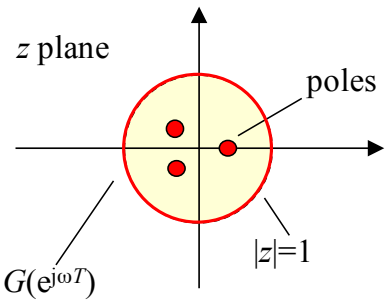
The Z-Transform $X(z)$ of a discrete-time sequence $x[k]$ is defined as:

$$X(z) \equiv \sum_{n=0}^{+\infty} x[n] \cdot z^{-n}$$

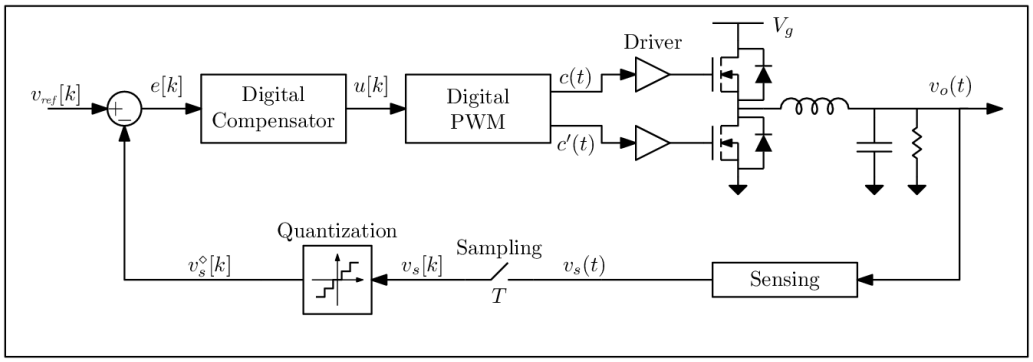
The Z-Transform plays for discrete time systems a role similar to that of the Laplace Transform for analog systems:

2) For a stable system, the poles of $G(z)$ are inside the unity circle

3) Evaluation of $G(z)$ along the unity circle gives the system's frequency response $G(e^{j\omega T})$



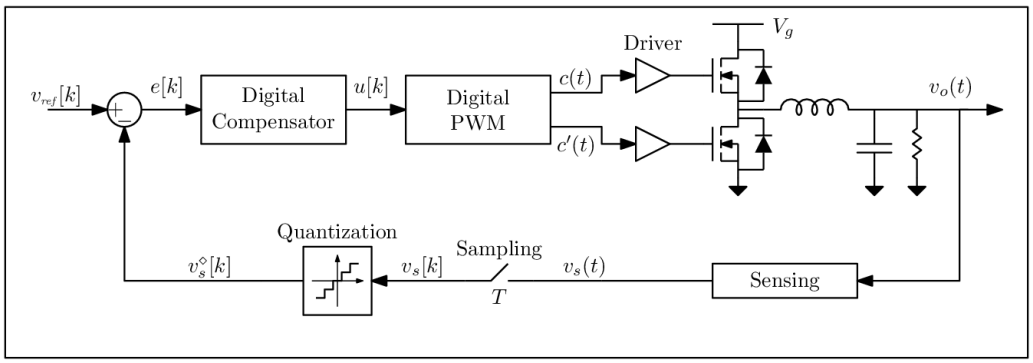
Example: Synchronous Buck Converter



- Converter output voltage is sensed, sampled and quantized into a digital signal $v_s^{\Diamond}[k]$.
- Sampling rate is $f_c = 1/T$. The most common choice is to set the control sampling rate equal to the converter switching rate:

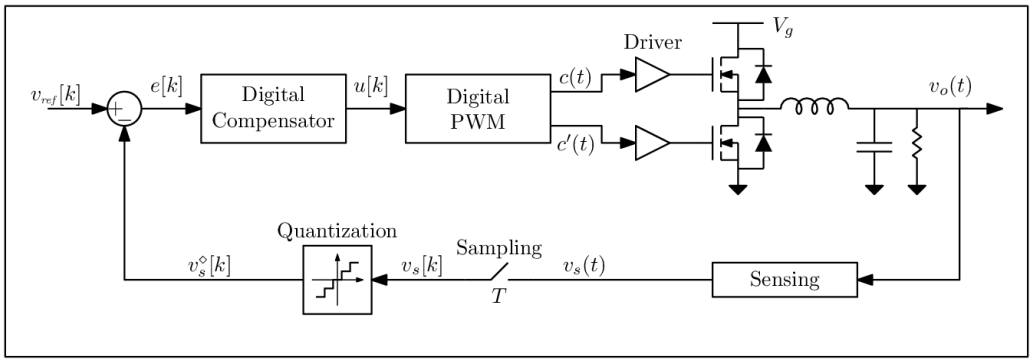
$$f_c = f_s$$

Example: Synchronous Buck Converter



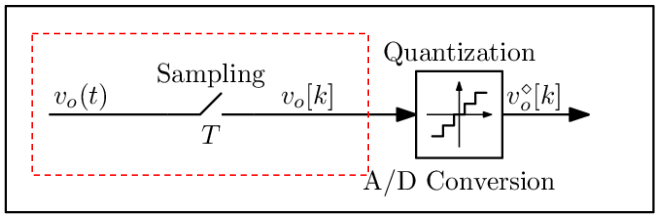
- Digital sequence $v_s^{\Diamond}[k]$ is compared with the control setpoint $v_{ref}[k]$, and the resulting *regulation error* $e[k]$ is processed by the digital compensator.
- The latter calculates, according to its internal control law, the control command $u[k]$ to be applied to the converter during the subsequent switching interval.

Example: Synchronous Buck Converter



- A **digital pulse width modulator (DPWM)** compares the digital control command $u[k]$ with an internal carrier $r(t)$, producing a pulse width-modulated output $c(t)$ with duty cycle $d[k]$.
- Generation of *dead times* – necessary in order to avoid cross-conduction of the converter switches – is implemented either by the DPWM itself or by the gate driving circuitry.

Analog to Digital Conversion: Sampling



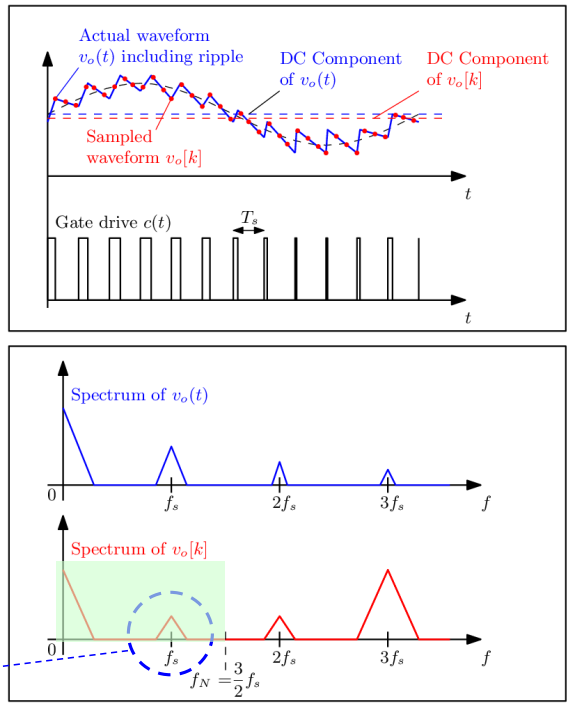
- Sampling is always synchronized with respect to the PWM carrier: sampling instants always occur at a fixed position with respect to the switching interval.
- Excluding sampling rates strictly smaller than the switching rate, let us assume the sampling period T is a fraction of the converter switching period T_s:

$$T = \frac{T_s}{n}$$

- Cases:
  - $T = T_s$ "single sampling"
  - $T < T_s$ "multisampling"

Sampling: $T < T_s$

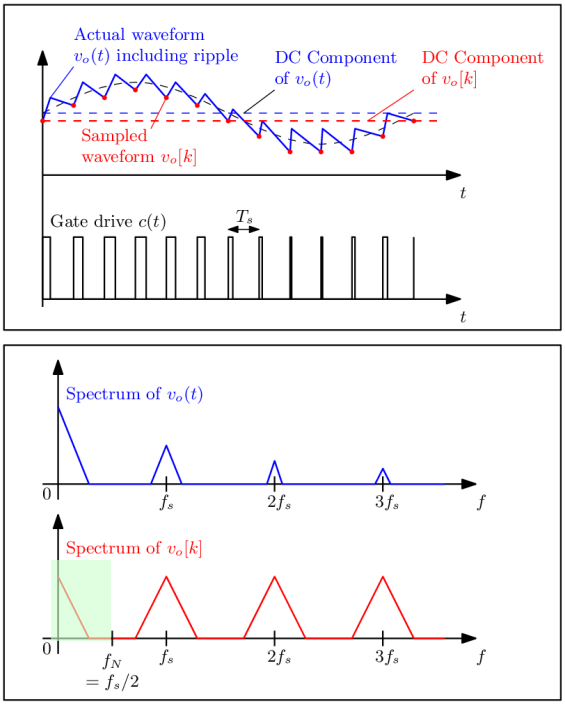
- Suppose the sampling period T is smaller than the switching period T_s. In the Figure, $T = T_s/3$
- The Nyquist rate f_N is equal to 3/2 of the switching rate f_s.
- Spectral aliasing due to sampling occurs around f=0 and around f=f_s.
- ➔ Aliased switching noise appears around f=f_s and requires digital filtering to be attenuated.
- The situation is similar to the analog case, in which high-frequency poles are purposely introduced in the compensator to attenuate switching harmonics.



Aliased
switching noise

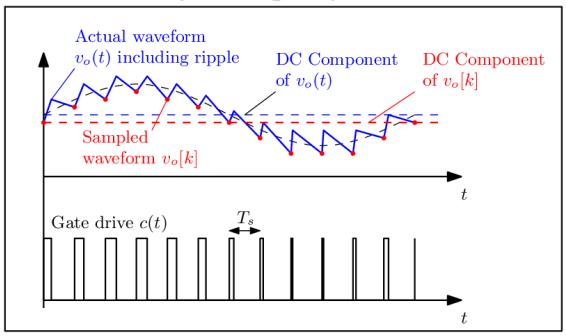
Sampling: $T = T_s$

- Suppose now that $T = T_s$, i.e. the sampling rate is equal to the converter switching rate.
- This corresponds to sampling the output signal once every switching period, as illustrated in the Figure.
- The Nyquist rate f_N is equal to one half the switching frequency.
- Spectral aliasing only occurs around f=0.
- ➔ No aliased switching noise appears below the Nyquist rate. No digital filtering is required.

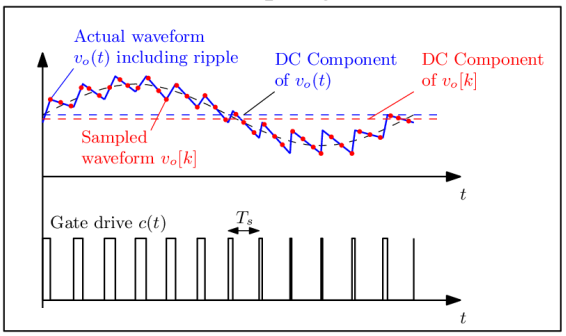


Single Sampling vs. Multisampling

Single sampling, $T = T_s$

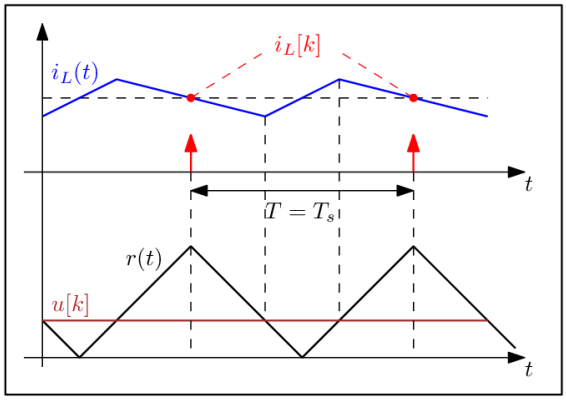


Multisampling, $T < T_s$



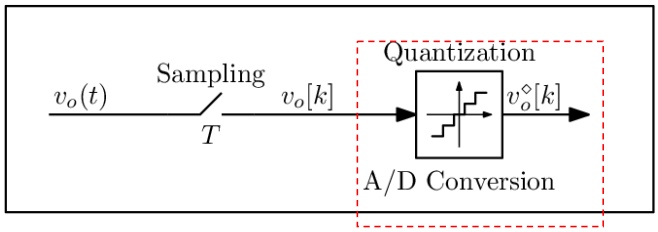
- In power electronics, a common and simple choice is to use a sampling frequency equal to the converter switching frequency.
- Increasing the sampling rate can however lead to superior dynamic performances in high-frequency dc-dc applications if a suitable filtering of the aliased noise is implemented.

Analog to Digital Conversion: Comments on $T = T_s$

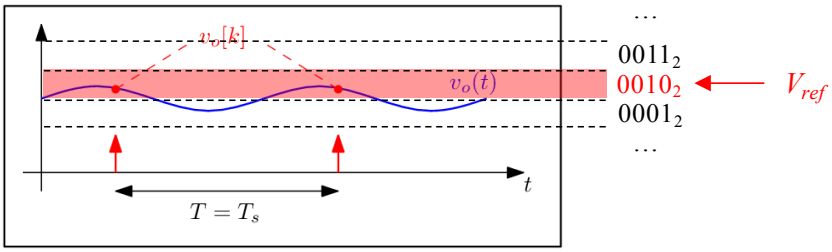


- Case of triangular ripple: sampling at the middle of the turn-on or turn-off interval exactly yields the average value, with no aliasing distortion.
- Example: sampling of inductor current in digital current control loops

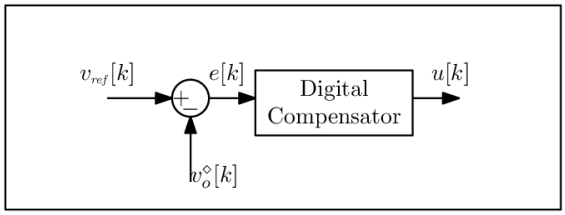
Analog to Digital Conversion: Quantization



- Output range is quantized into a number of voltage intervals, sometimes called *bins*, each identified by a binary code
- In regulation applications, the *zero error bin* represents the voltage interval defining the reference value:



Digital Compensator



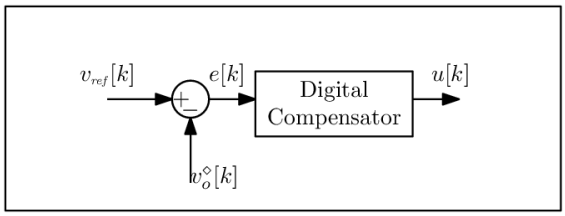
- The digital compensator updates $u[k]$ on a switching cycle basis from the voltage error $e[k] = v_{ref}[k]\text{-}v_o^{\Diamond}[k]$ and from its internal state.
- As long as the digital compensator is linear and time-invariant, it is always governed by a linear, constant coefficients *difference equation*:

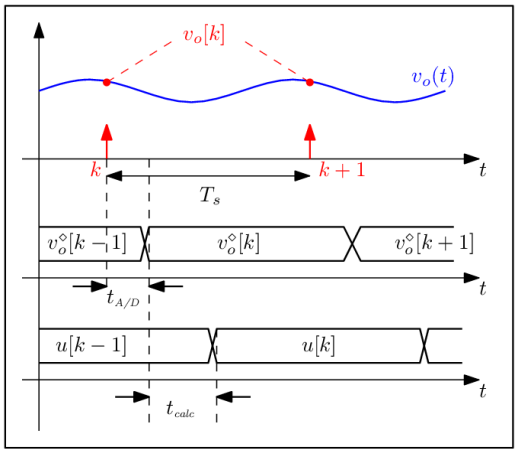
$$u[k] = -a_1 \cdot u[k-1] - a_2 \cdot u[k-2] - \ldots - a_N \cdot u[k-N] + \\ + b_0 \cdot e[k] + b_1 \cdot e[k-1] + b_2 \cdot e[k-2] + \ldots + b_M \cdot e[k-M]$$

- In the z-domain, the compensator transfer function is

$$G_c(z) = \frac{\hat{u}(z)}{\hat{e}(z)} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_M z^{-M}}{1 + a_1 z^{-1} + a_2 z^{-2} + \ldots + a_N z^{-N}}$$

Digital Compensator





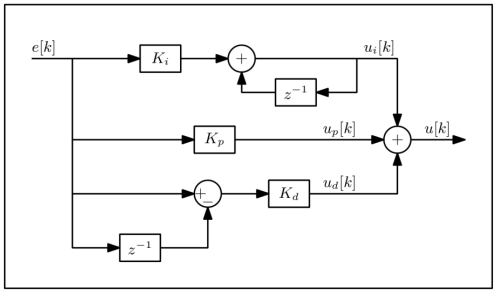
- The above equations assume that $u[k]$ is immediately available at the compensator output as soon as $e[k]$ updates.
- In practice, calculation of $u[k]$ takes a certain computational delay t_{calc}.

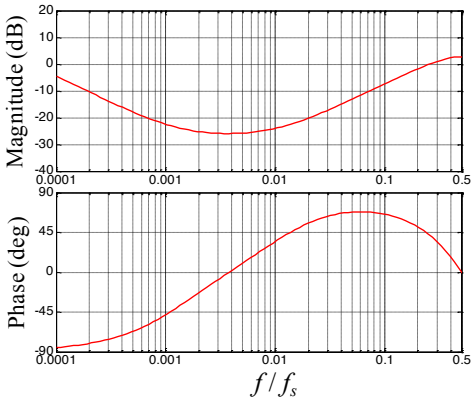
Digital PID Compensators

- An important class of linear compensators is that of Proportional-Integral-Derivative (PID) compensators, having a transfer function of the form:

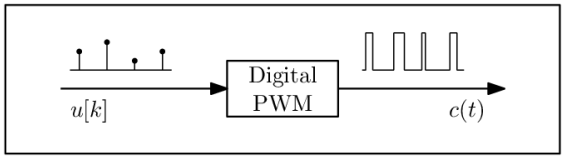
$$G_c(z) = \frac{K_i}{1-z^{-1}} + K_p + K_d \cdot \left(1 - z^{-1}\right)$$

- The Figure illustrates a block diagram example of a digital PID and exemplifies magnitude and phase Bode diagrams of its frequency response.



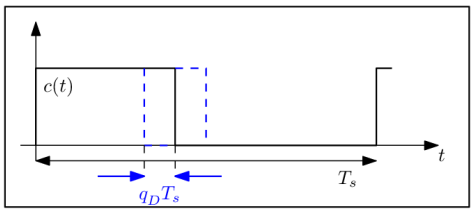


Digital Pulse Width Modulation



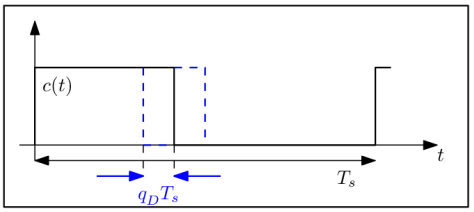
- Function: generate a square wave with duty cycle D proportional to the input signal $u[k]$.

- A digital PWM is only capable of generating a *discrete* set of duty cycles. In other words, duty cycle quantization occurs.



- The smallest duty cycle variation q_D the modulator is capable of determines its *resolution*.

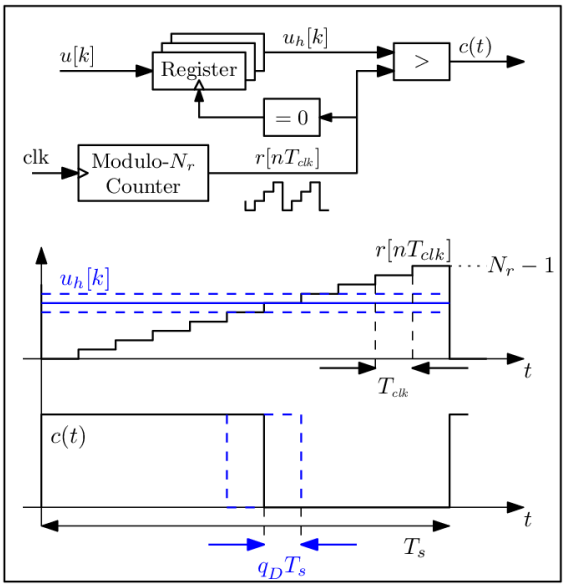
Digital Pulse Width Modulation



- Duty cycle quantization induces a corresponding quantization $q_{o,DPWM}$ of the attainable output voltage values. For a Buck converter:

$$V_{out} = D \cdot V_g \quad \Rightarrow \quad q_{o,DPWM} = q_D \cdot V_g$$

Example: Counter-Based DPWM



- Very simple DPWM implementation which imitates the analog one.
- Duty cycle: $D = \frac{U}{N_r}$

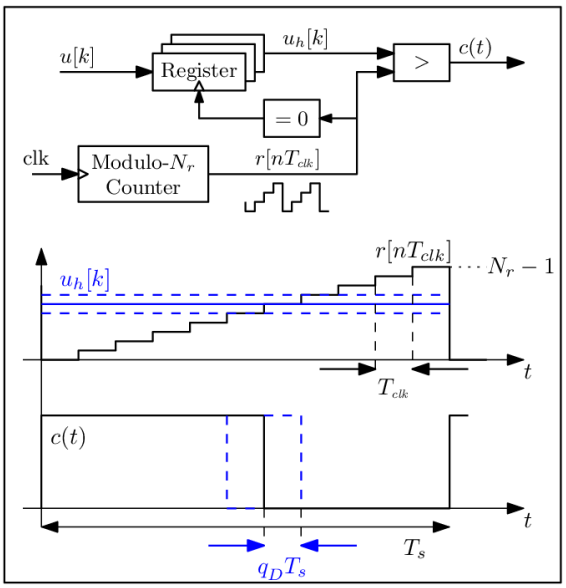
  where $N_r = f_{clk} / f_s$.
- Time resolution is determined by clock period T_{clk}
- Minimum duty cycle variation:

$$q_D = \frac{1}{N_r}$$

- Corresponding output voltage quantization:

$$q_{o,DPWM} = \frac{V_g}{N_r}$$

Example: Counter-Based DPWM



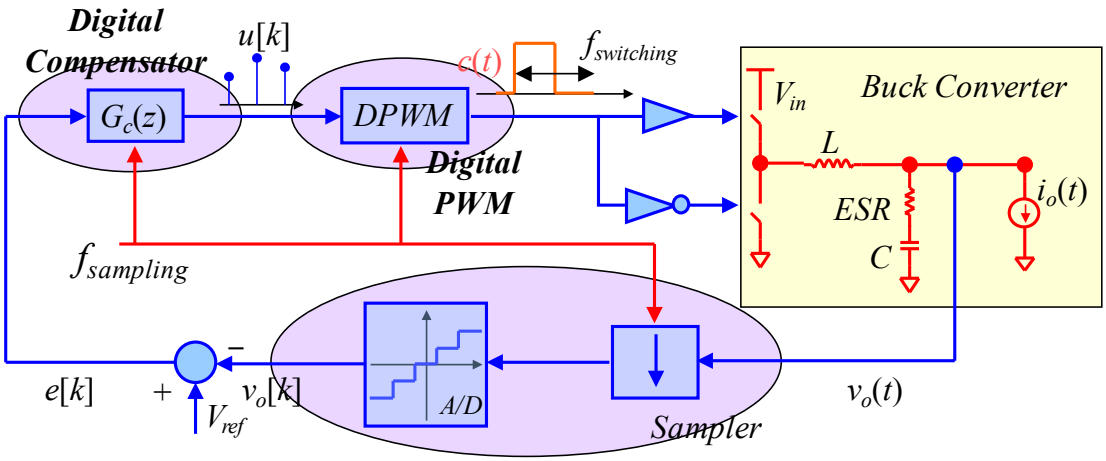
- For a given switching rate f_s, the clock frequency f_{clk} required to achieve a resolution of n bits is:

$$f_{clk} = f_s \cdot 2^n$$

- ➔ f_{clk} is an exponential function of the number of bits.
- ➔ The counter-based solution is only practical for small resolutions or small switching rates.
- Different DPWM architectures are needed for large resolutions and higher switching rates.

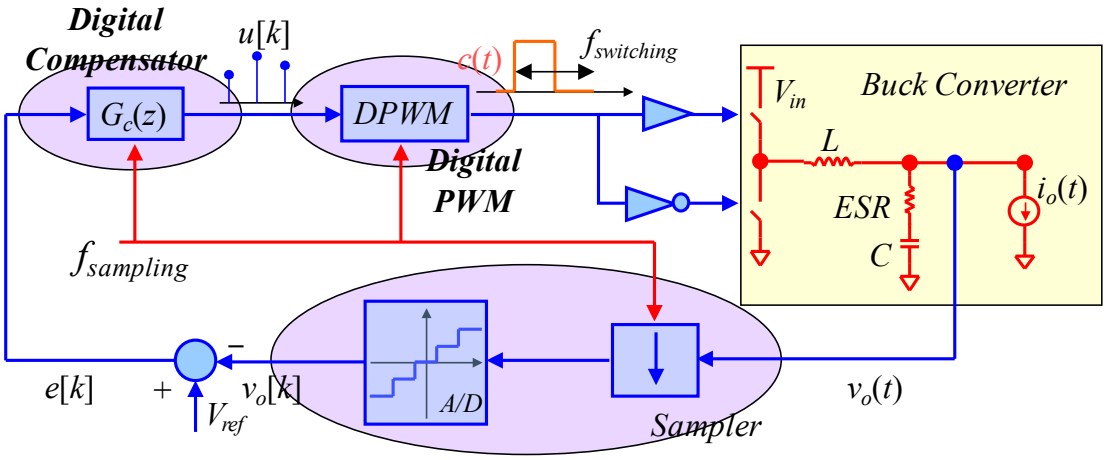
Part II
Modulation Delay, Basic Modeling Techniques and Controller Design

Digital Voltage-Mode Control



- Control operation:
  - The converter output voltage is sampled and quantized
  - A discrete-time compensator processes the error $e[k]$ and outputs the modulating signal $u[k]$
  - A digital pulse-width modulator generates the PWM signal $c(t)$

Digital Voltage-Mode Control



- Loop dynamic performances are constrained by the total loop delay t_d, sum of the following contributions:
  - A/D conversion delay
  - Computational delay
  - Gate drive propagation delay
  - **Modulator delay**

?

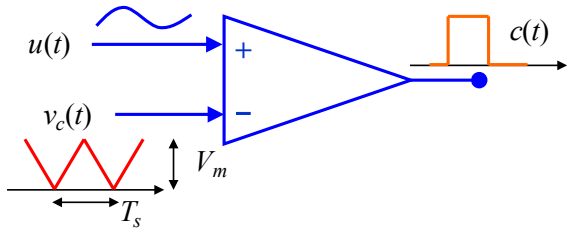
Small-Signal Modeling of Pulse Width Modulators

Three families of PWM modulators can be identified:

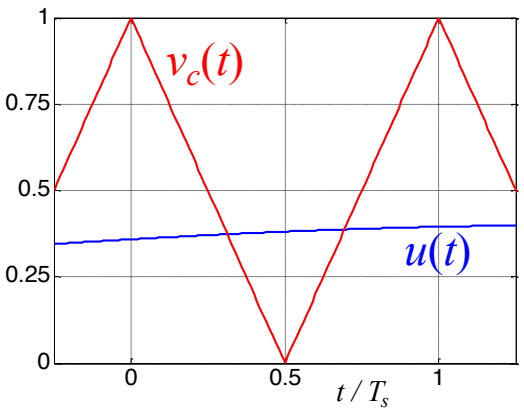
Naturally sampled modulators

Multiple sampled modulators

Uniformly sampled (or single-sampled) modulators



Process an *analog* modulating signal $u(t)$. They are commonly employed in traditional analog PWM control



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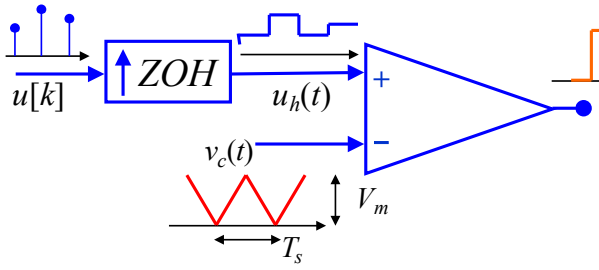

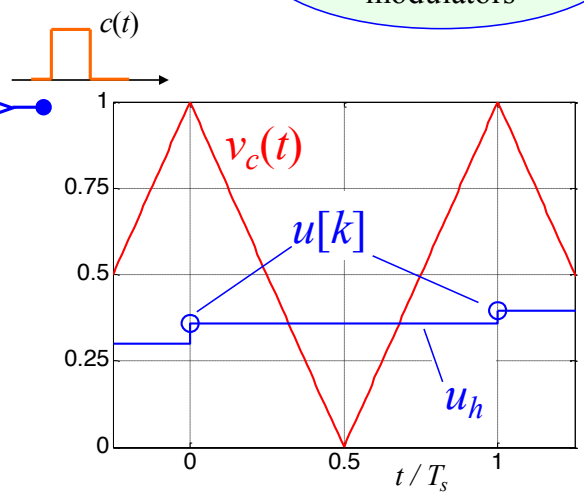

Process a *discrete-time* modulating signal $u[k]$, updated once per switching period: $f_{sampling} = f_{switching}$

Small-Signal Modeling of Pulse Width Modulators

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Naturally sampled modulators

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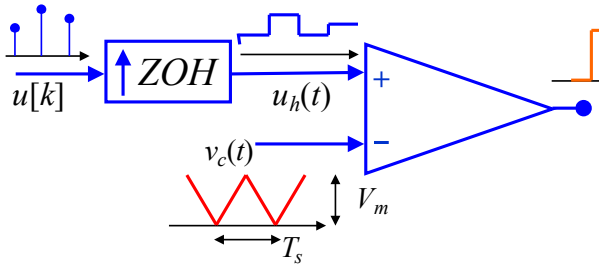
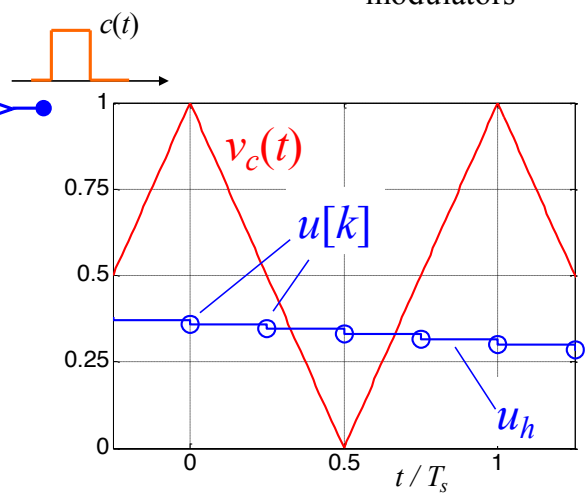
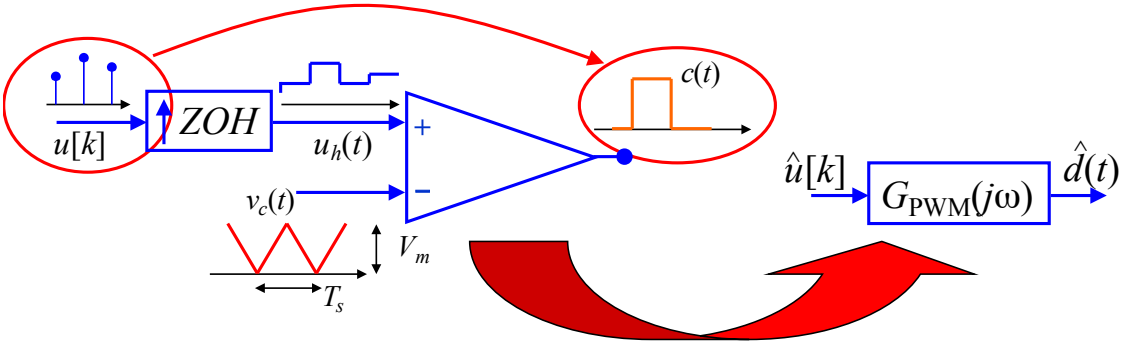




Process a *discrete-time* modulating signal $u[k]$, updated N times per switching period: $f_{sampling} = N \cdot f_{switching}$

Small-Signal Modeling of Pulse Width Modulators

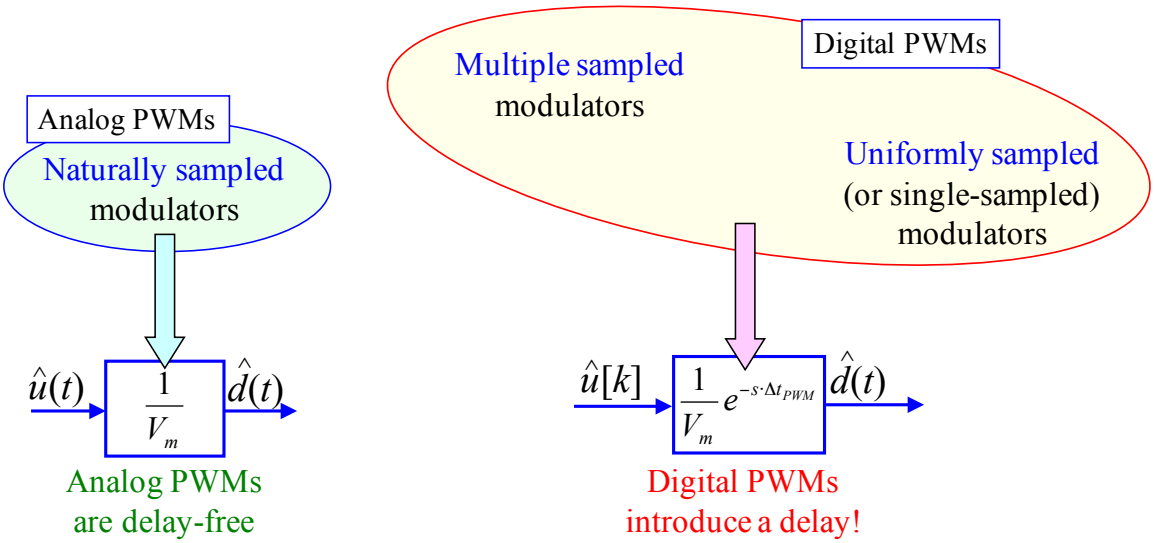


Finding the small-signal frequency response of a pulse-width modulator means [61]:

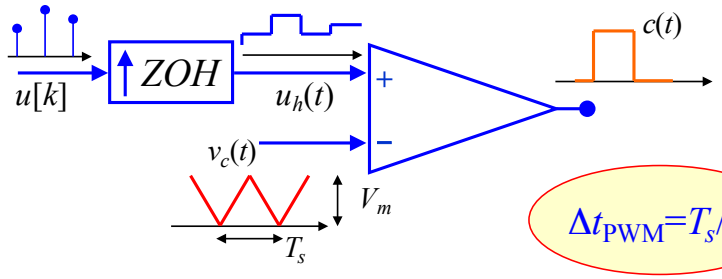
1. Applying a small sinusoidal perturbation at frequency ω to the modulating signal u
2. Calculating the Fourier component $d(t)$ of the PWM output $c(t)$ at frequency ω
3. Calculating the amplitude/phase relationship $G_{PWM}(j\omega)$ between d and u at frequency ω

Small-Signal Modeling of Pulse Width Modulators

Small-signal PWM analysis – summary of main results

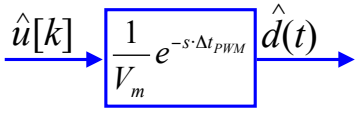


Physical Origin of PWM Delay

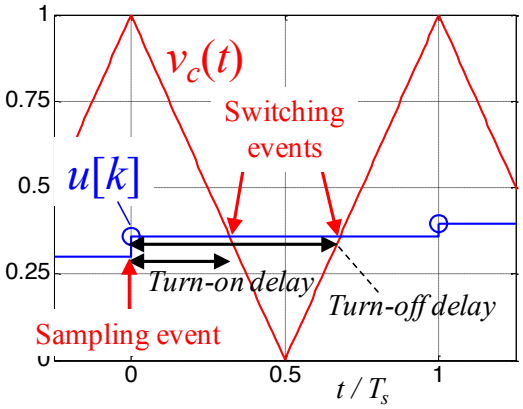


$\Delta t_{PWM}=T_s/2$

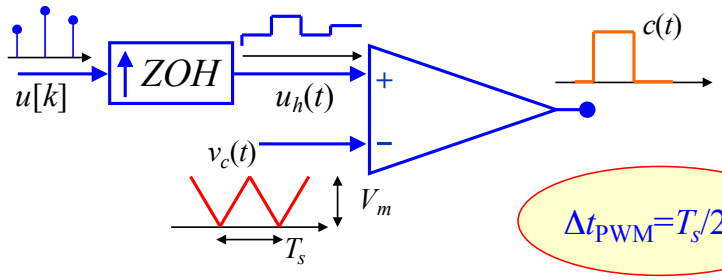
Uniformly sampled modulators:
$d(t)$ is *delayed* with respect to $u[k]$:



Physical origin of such delay is the difference between the sampling instant and the switching instants



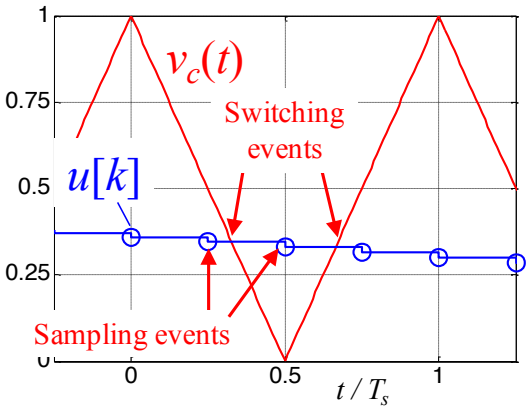
Physical Origin of PWM Delay



$\Delta t_{PWM}=T_s/2N$

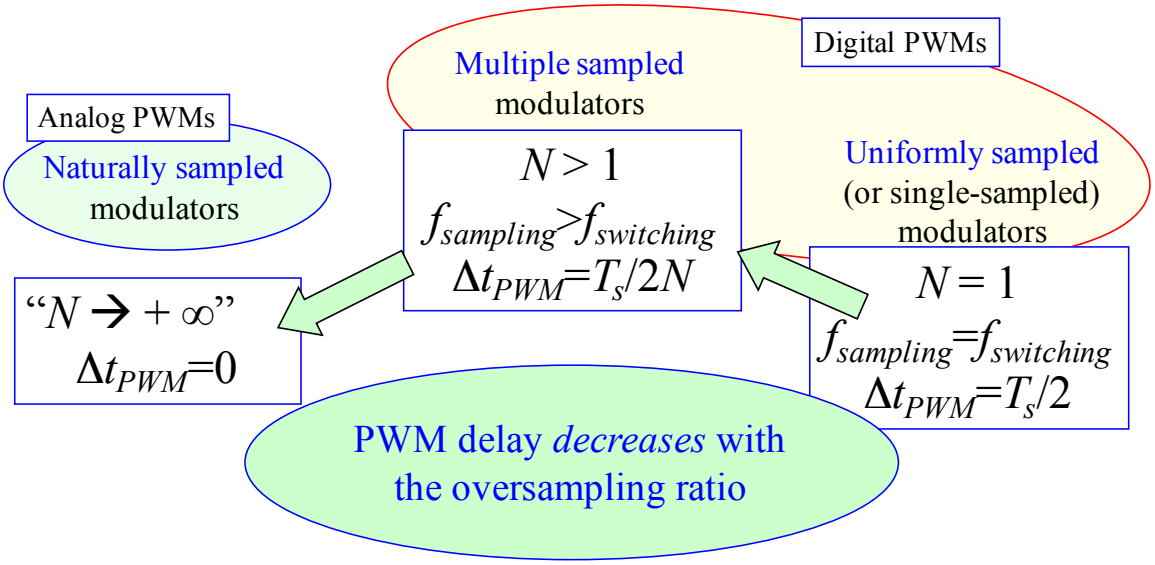
Multiple sampled modulators:
$d(t)$ still delayed with respect to $u[k]$, but difference between sampling and switching event is reduced.

➔ In a multisampled modulator, delay is reduced because of the increased sampling rate.



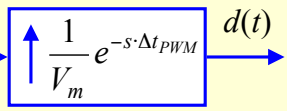
Modeling of Pulse Width Modulators: Summary

$N = f_{sampling}/f_{switching}$ represents the number of times the modulating signal is updated within the switching period

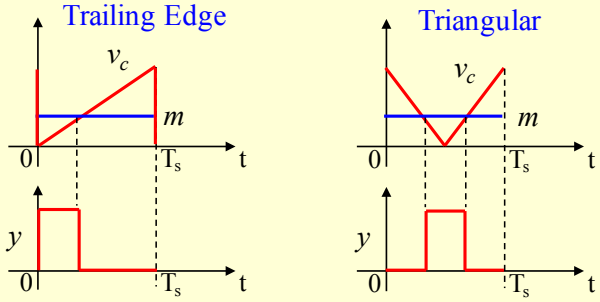


Modeling of Pulse Width Modulators: Summary

Results for the triangular and trailing edge modulators



Trailing edge modulators exhibit a delay that depends on the converter steady state duty ratio D



Uniformly Sampled:

$\Delta t_{PWM} = D \cdot T_s$

$\Delta t_{PWM} = \frac{T_s}{2}$

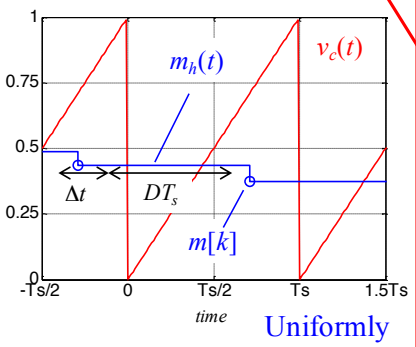
Multiple Sampled:

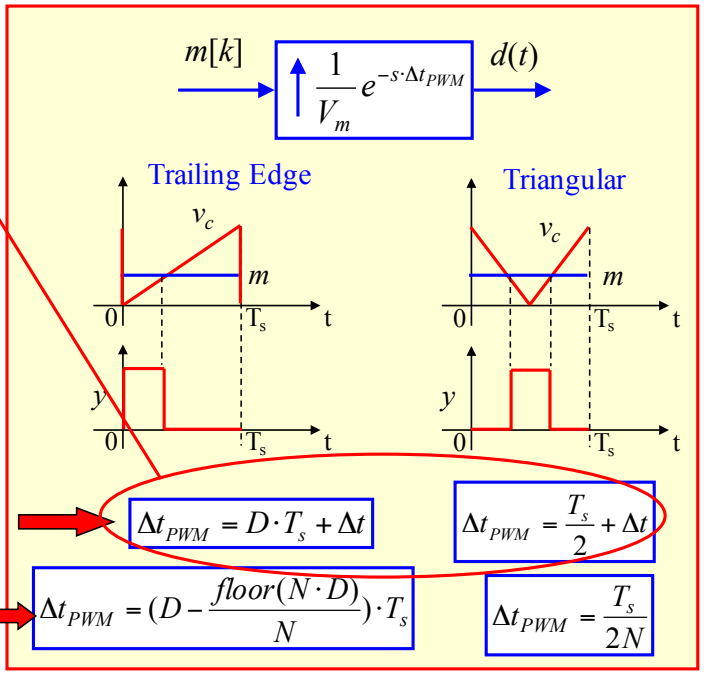
$\Delta t_{PWM} = (D - \frac{floor(N \cdot D)}{N}) \cdot T_s$

$\Delta t_{PWM} = \frac{T_s}{2N}$

Modeling of Pulse Width Modulators: Summary

Note: add Δt whenever the sampling occurs Δt seconds before the beginning of the switching cycle





Uniformly Sampled:

$$\Delta t_{PWM} = D \cdot T_s + \Delta t$$

$$\Delta t_{PWM} = \frac{T_s}{2} + \Delta t$$

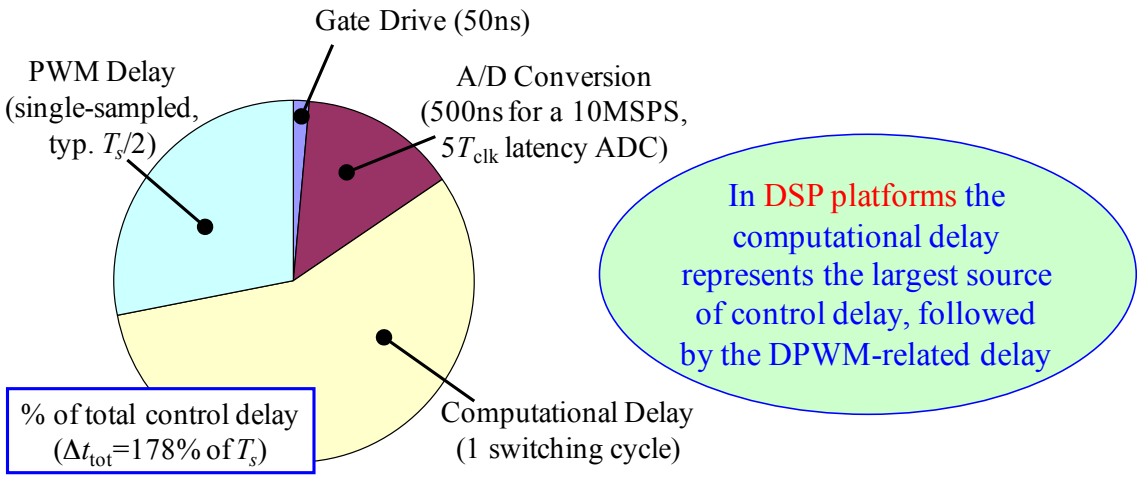
Multiple Sampled:

$$\Delta t_{PWM} = (D - \frac{floor(N \cdot D)}{N}) \cdot T_s$$

$$\Delta t_{PWM} = \frac{T_s}{2N}$$

Sources of Control Delays: DSP-based Controller

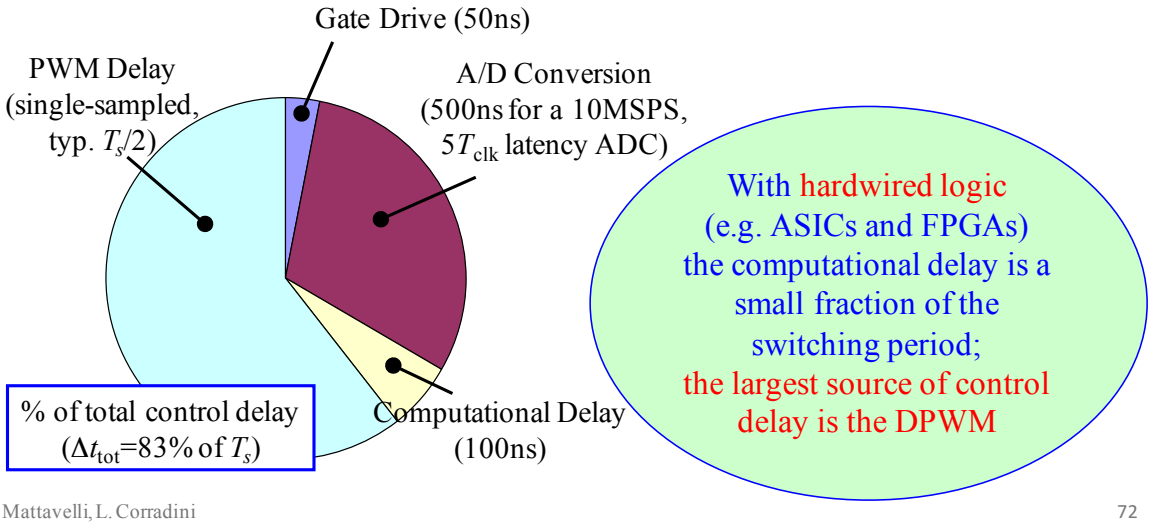
- Example: $f_{switching} = 500$ kHz application, $f_c = f_s/10$ control bandwidth
- Relative importance of various control delays:



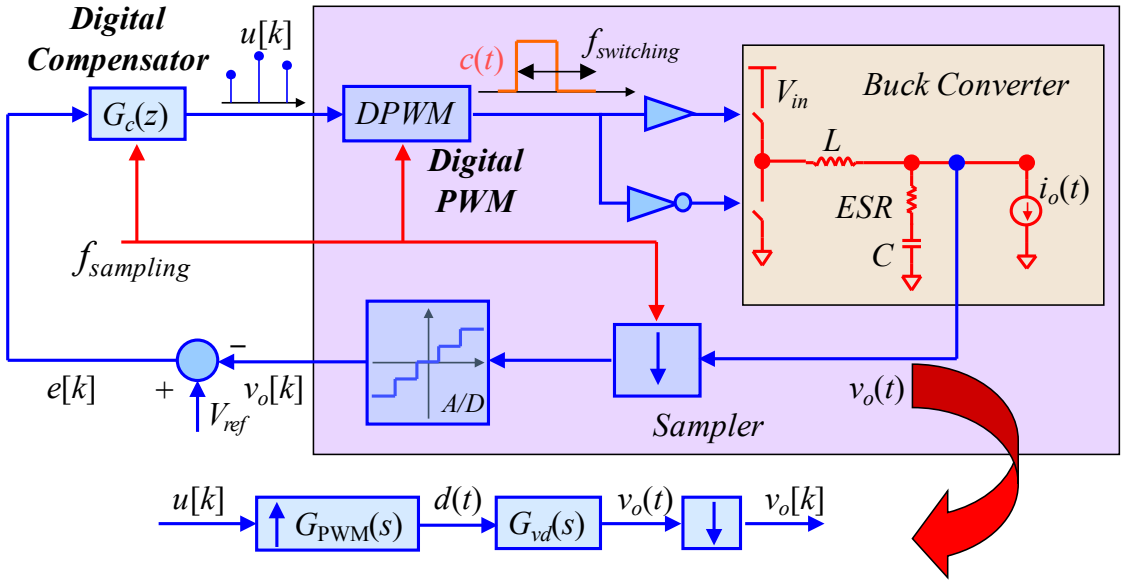
In DSP platforms the computational delay represents the largest source of control delay, followed by the DPWM-related delay

Sources of Control Delays: Hardwired Controller

- Example: $f_{\text{switching}} = 500$ kHz application, $f_c = f_s/10$ control bandwidth
- Relative importance of various control delays:

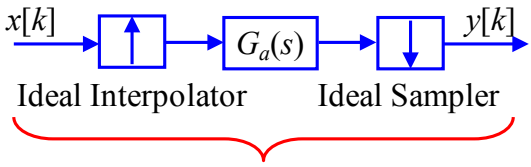


z-Domain modeling of the voltage mode control loop

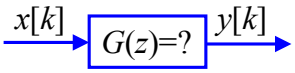


Discrete-Time Equivalent of a Continuous-Time System

Let $G_a(s)$ be the transfer function of an analog system driven by a stream of modulated Dirac pulses and followed by an ideal sampler;



The impulse response $g[k]$ of the discrete time equivalent system is T times the sampled version of the continuous time impulse response:

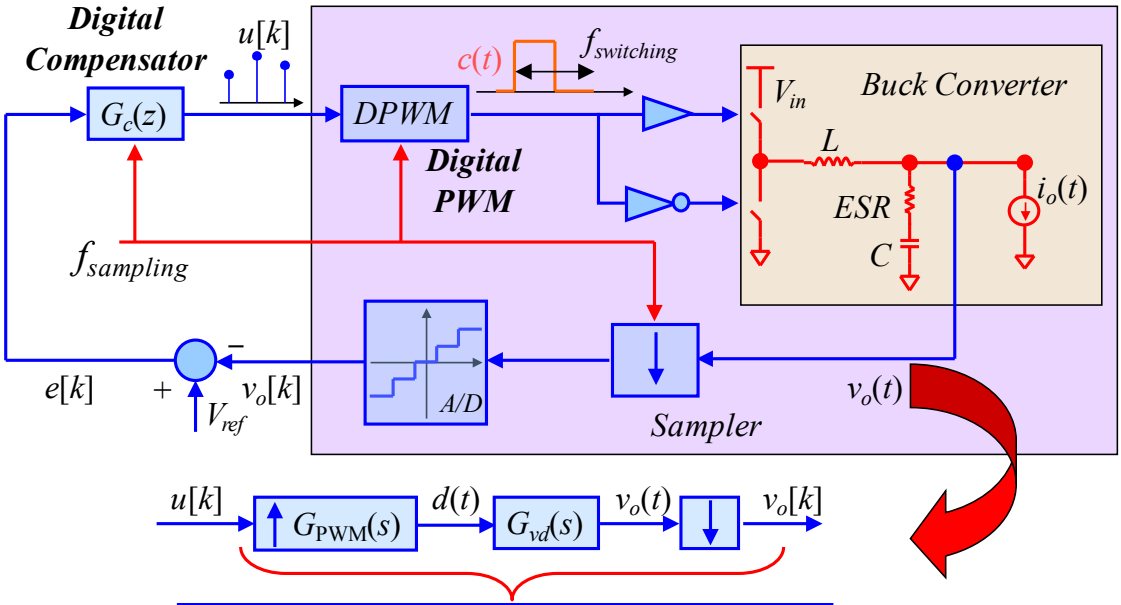


$$g[k] = T \cdot g_a(t=kT) \Rightarrow G(z) = T \cdot Z_T[G_a(s)]$$

, where we defined:

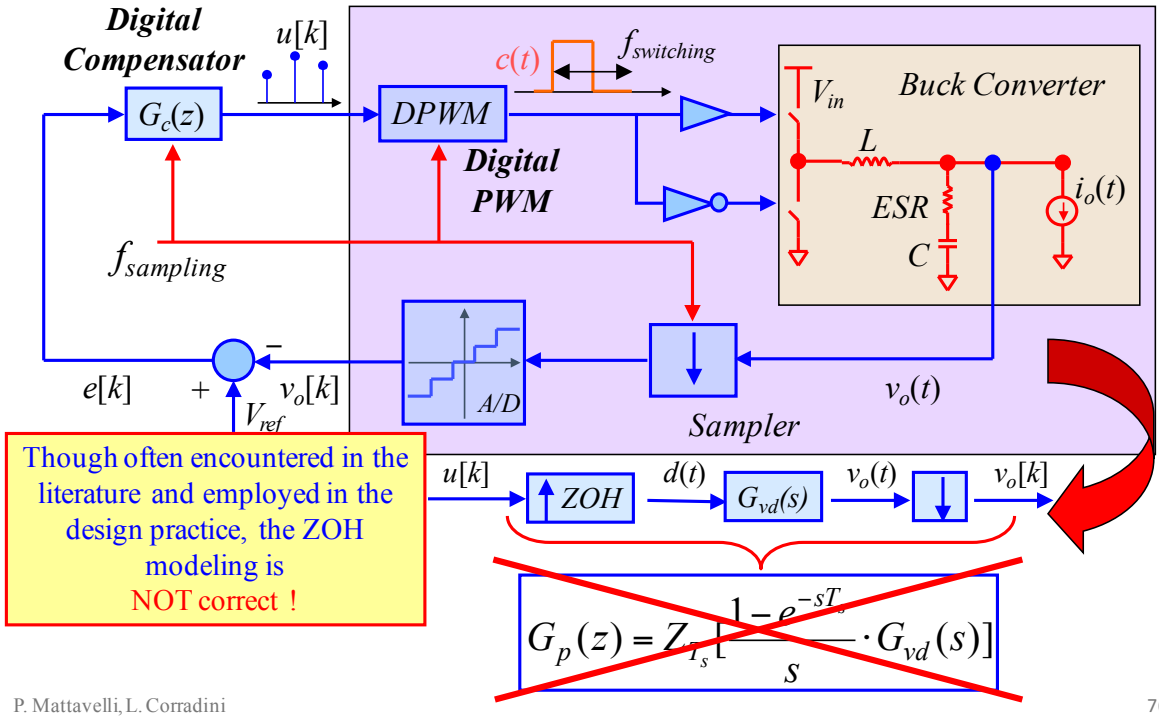
$$Z_T[G_a(s)] \equiv \sum_{n=0}^{+\infty} g_a(t = nT) \cdot z^{-n}$$

z-Domain modeling of the voltage mode control loop



$$G_p(z) \equiv \frac{V_o(z)}{U(z)} = T_s \cdot Z_{T_s}[G_{PWM}(s) \cdot G_{vd}(s)]$$

A Common Misconception: Zero-Order Hold Modeling



z-Domain Modeling of the Voltage Mode Control Loop

Design example: 12 V–5 V, 50 W synchronous Buck converter with triangular modulation

L=2 μH, r_L=2 mΩ, C=1 mF, ESR=1 mΩ, $f_{switching}$=200 kHz=$f_{sampling}$

Let us derive the z-domain discrete time equivalent $G_p(z)$:

1) Write the control-to-output transfer function of the power converter:

$$G_{vd}(s) = \frac{1 + s \cdot ESR \cdot C}{1 + s \cdot (r_L + ESR)C + s^2 \cdot LC} V_{in}$$

2) Write the PWM transfer function:

$$G_{PWM}(s) = \frac{e^{-s\frac{T_s}{2}}}{V_m}$$

3) Discretization:

$$G_p(z) = T_s \cdot Z_{T_s}[\frac{(1 + s \cdot ESR \cdot C) \cdot V_{in}}{1 + s \cdot (r_L + ESR)C + s^2 \cdot LC} \cdot \frac{e^{-s\frac{T_s}{2}}}{V_m}]$$

z-Domain Modeling of the Voltage Mode Control Loop

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Few Matlab instructions will do the job:

```
s=tf('s');
Gvd=Vin*(1+s*ESR*C)/(1+s*(rL+ESR)*C)+s^2*L*C);
set(Gvd,'inputdelay',Ts/2);
Gp=Ts*c2d(Gvd,Ts,'imp');
```

The "impulse response discretization" option ('imp') implements the operator $Z_{Ts}[\cdot]$.

z-Domain Modeling of the Voltage Mode Control Loop

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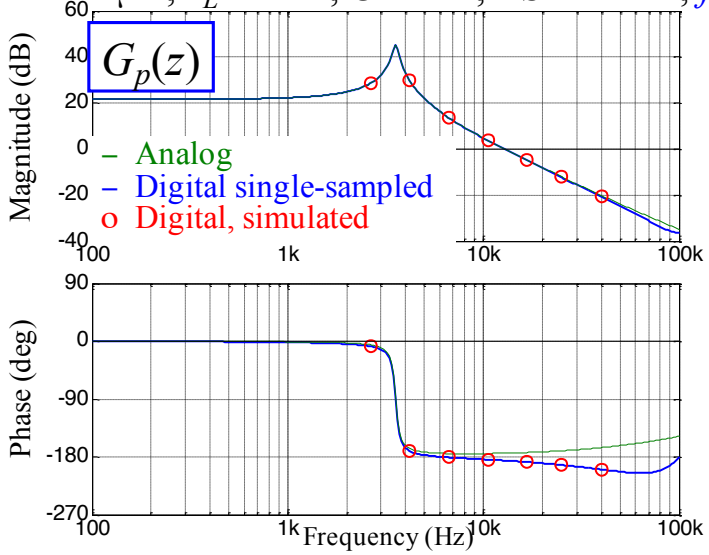

Comparison between digital and analog control-to-output transfer function reveals the larger phase lag of the former, due to the PWM delay

Bandwidth limitation!

PWM-related delays may severely degrade achievable performances in digitally controlled SMPS!

z-Domain Modeling of the Voltage Mode Control Loop

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…ular modulation

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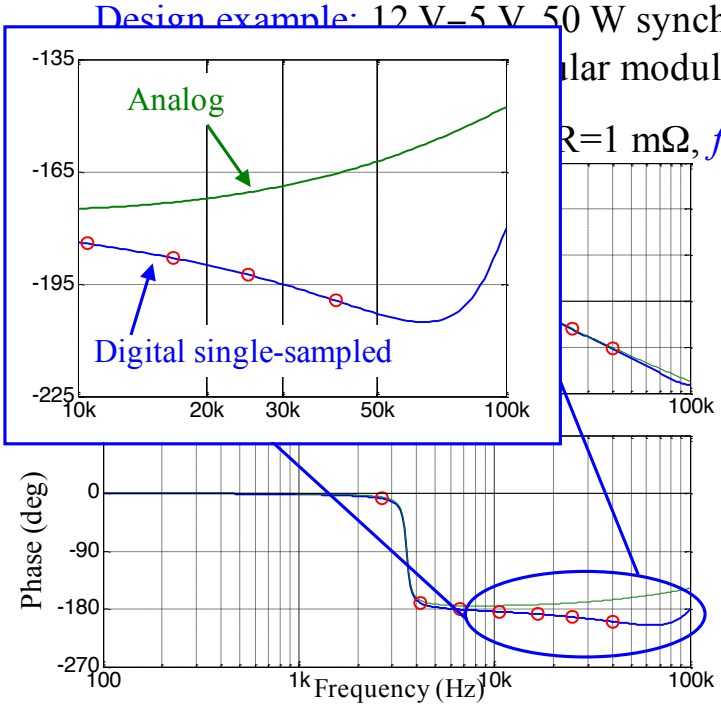

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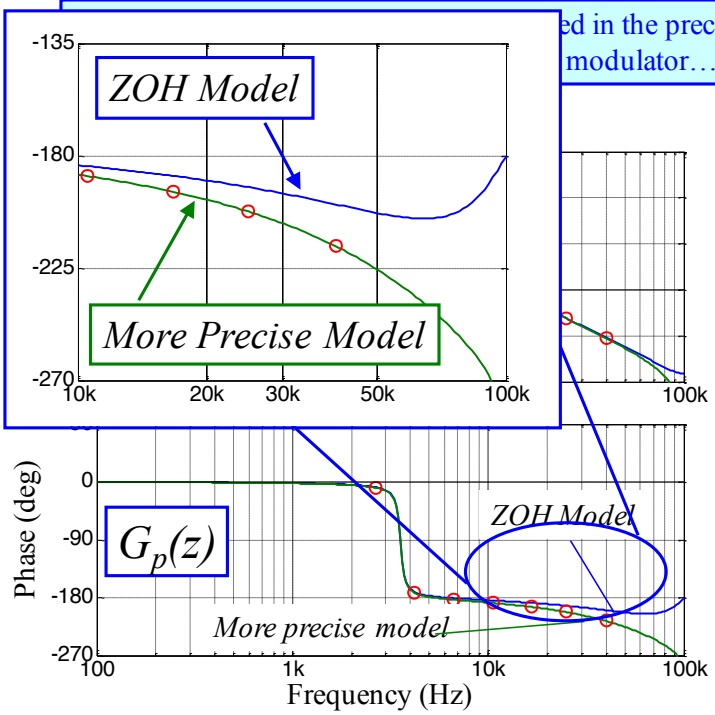
A Common Misconception: Zero-Order Hold Modeling

…ed in the preceding example, rather than a …modulator…



…the ZOH modeling approach fails to correctly predict the converter phase behavior

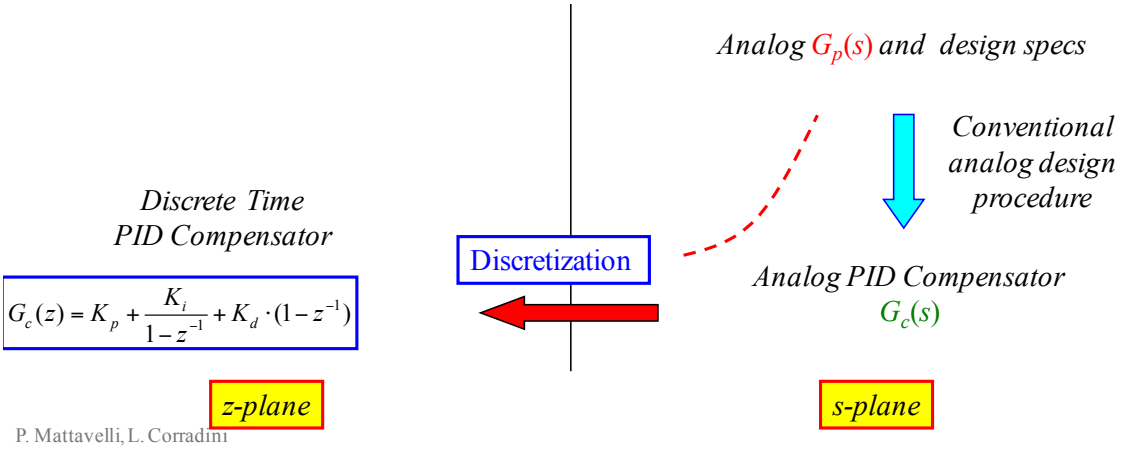
Reason: for trailing edge modulations, the PWM delay depends on the steady state duty ratio D. The ZOH model does not describe this effect!

Controller Design Using Continuous-Time Modeling

Design example: 12 V–5 V, 50 W synchronous Buck converter with triangular modulation

L=2 μH, r_L=2 mΩ, C=1 mF, ESR=1 mΩ, $f_{switching}$=200 kHz=$f_{sampling}$

Another popular design method is the *s*-domain design of the compensator followed by its discretization:

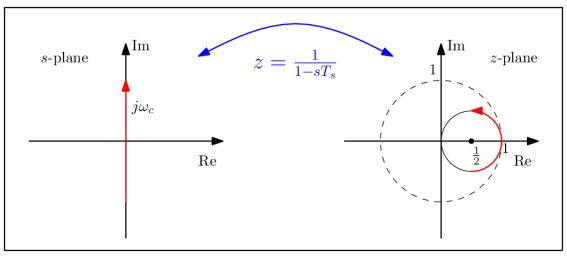


Euler Discretization

- It is based on the map:

$$s = \frac{1-z^{-1}}{T_s} \quad \Leftrightarrow \quad z = \frac{1}{1-sT_s}$$

- Such transformation maps the Re[*s*]<0 half-plane inside the unit circle in the *z*-plane. Such property guarantees that a stable pole in the *s*-plane is mapped into a stable pole in the *z*-plane.
- In particular, the Re[*s*]<0 half-plane transforms into the disk centered at (½ , 0) and of radius ½, as illustrated in the Figure:



Euler Discretization of a Continuous-Time PID

- Let

$$D_c(s) = K_p + \frac{K_i}{s} + sK_d$$

be the transfer function of a continuous-time PID compensator, K_p, K_i and K_d being the proportional, integral and derivative gains respectively. Assume these gains have already be determined.

- Euler discretization of $D_c(s)$ is

$$G_c(z) = D_c\left(\frac{1-z^{-1}}{T_s}\right) = K_p + \frac{K_i T_s}{1-z^{-1}} + \frac{K_d}{T_s}\cdot(1-z^{-1})$$

- Coefficients $K_{p,d}, K_{i,d}$ and $K_{d,d}$ of the discrete-time PID are

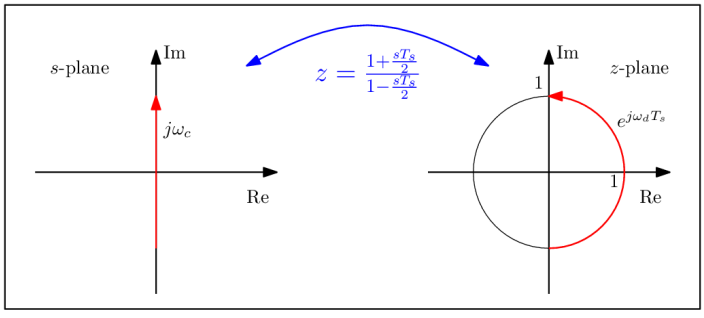
$$\begin{aligned} K_{p,d} &= K_p \\ K_{i,d} &= K_i T_s \\ K_{d,d} &= \frac{K_d}{T_s} \end{aligned}$$

Tustin Discretization

- It is based on the bilinear map

$$s = \frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}} \quad \Leftrightarrow \quad z = \frac{1+s\frac{T_s}{2}}{1-s\frac{T_s}{2}}$$

- Such transformation maps the Re[s]<0 half-plane into the $|z|<1$ unit disk, and the imaginary axis $s = jw_c$ into the unit circle $z=\exp(jw_d T_s)$:



Tustin Discretization of a Continuous-Time PID

- Let

$$D_c(s) = K_p + \frac{K_i}{s} + sK_d$$

be the transfer function of a continuous-time PID compensator, K_p, K_i and K_d being the proportional, integral and derivative gains respectively. Assume these gains have already be determined.

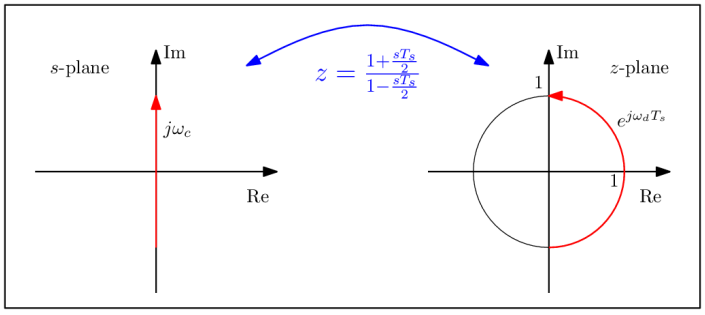
- Tustin discretization of $D_c(s)$ is

$$G_c(z) = D_c\left(\frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}}\right) = K_p + \frac{K_i T_s}{2}\frac{1+z^{-1}}{1-z^{-1}} + \frac{2K_d}{T_s}\frac{1-z^{-1}}{1+z^{-1}}$$

- Coefficients $K_{p,d}, K_{i,d}$ and $K_{d,d}$ of the discrete-time PID are

$$K_{p,d} = K_p$$
$$K_{i,d} = \frac{K_i T_s}{2}$$
$$K_{d,d} = \frac{2K_d}{T_s}$$

Tustin Discretization



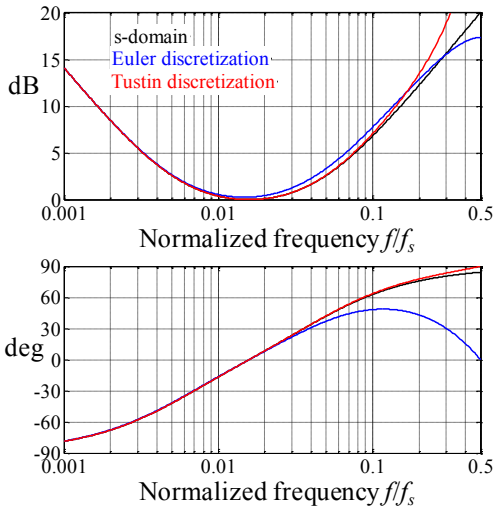
- If ω_c is the angular frequency in the s-plane, the angular frequency ω_d in the z–plane is

$$\omega_d = \frac{2}{T_s}\arctan\left(\frac{\omega_c T_s}{2}\right)$$

- This relationship describes a **frequency axis distortion** which must sometimes be compensated for when designing the analog controller.

Distortion in the Euler and Tustin Discretizations

- Neither the Euler nor the Tustin discretization method allow to exactly replicate the *s*-domain PID frequency response in the *z*-domain.
- As exemplified in the figure, discrepancy between *s*-domain and *z*-domain PID frequency responses becomes more and more severe as the frequency increases.
- The Euler discretization introduces a significant phase response error beyond one twentieth of the switching rate.
- The Tustin discretization provides a more accurate representation of the desired frequency response, typically to within one tenth of the switching rate.



Controller Design Using Discretization-Based Modeling

Design example: 12 V–5 V, 50 W synchronous Buck converter with triangular modulation

L=2 μH, r_L=2 mΩ, C=1 mF, ESR=1 mΩ, $f_{switching}$=200 kHz=$f_{sampling}$

Bilinear transform design method:

Uncompensated Loop Gain $G_p(z)$ *and design specs*

$$z(w) = \frac{1+\frac{wT_s}{2}}{1-\frac{wT_s}{2}}$$

"Analog" equivalent $G_p(z(w))$ *and design specs*

Conventional analog design procedure

It does NOT involve any approximation!

Discrete Time PID Compensator

$$G_c(z) = K_p + \frac{K_i}{1-z^{-1}} + K_d \cdot (1-z^{-1})$$

$$w(z) = \frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}}$$

"Analog" PID Compensator $G_c(w)$

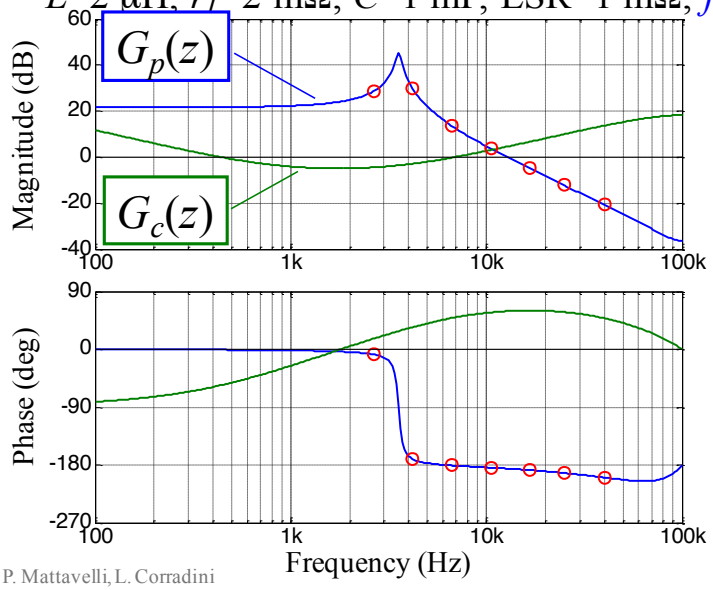
z-plane

w-plane

z-Domain Modeling of the Voltage Mode Control Loop

Design example: 12 V–5 V, 50 W synchronous Buck converter with triangular modulation

L=2 μH, r_L=2 mΩ, C=1 mF, ESR=1 mΩ, $f_{switching}$=200 kHz=$f_{sampling}$



Compensator design: a digital PID compensator $G_c(z)$ has been designed to achieve a 20 kHz closed-loop bandwidth with a 50° phase margin

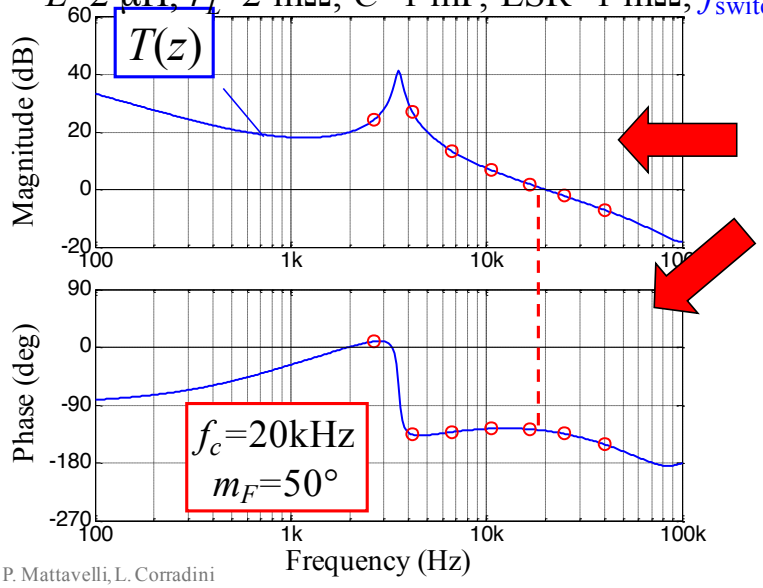
Many z-domain compensator design approaches exist.

The bilinear transform method was employed for this design.

z-Domain Modeling of the Voltage Mode Control Loop

Design example: 12 V–5 V, 50 W synchronous Buck converter with triangular modulation

L=2 μH, r_L=2 mΩ, C=1 mF, ESR=1 mΩ, $f_{switching}$=200 kHz=$f_{sampling}$



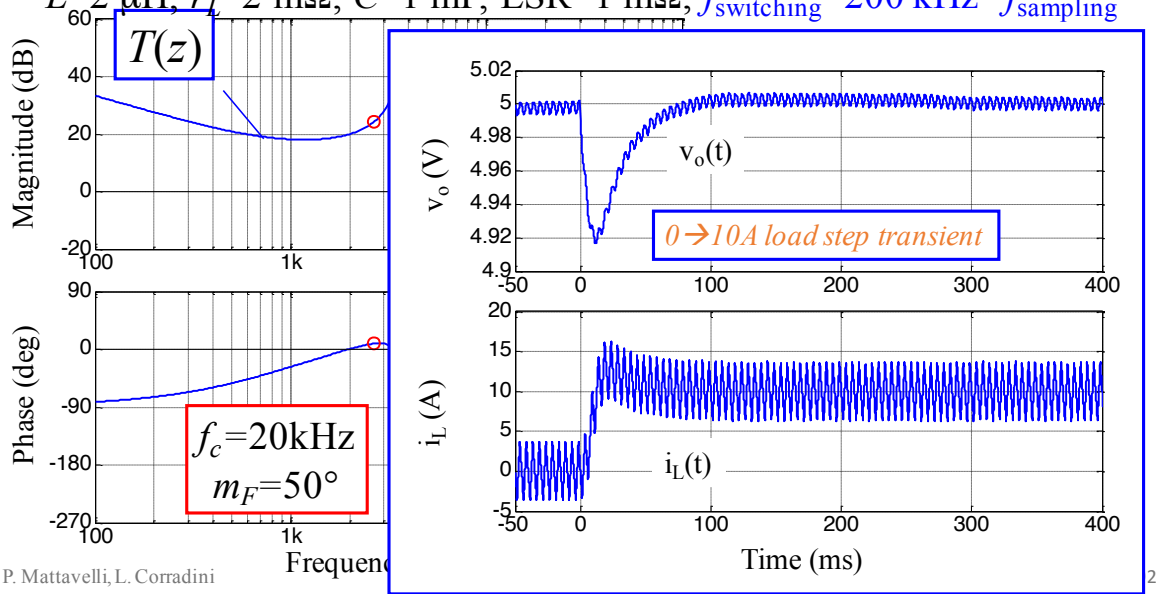
z-Domain loop gain

$T(z) = G_c(z) \cdot G_p(z)$

z-Domain Modeling of the Voltage Mode Control Loop

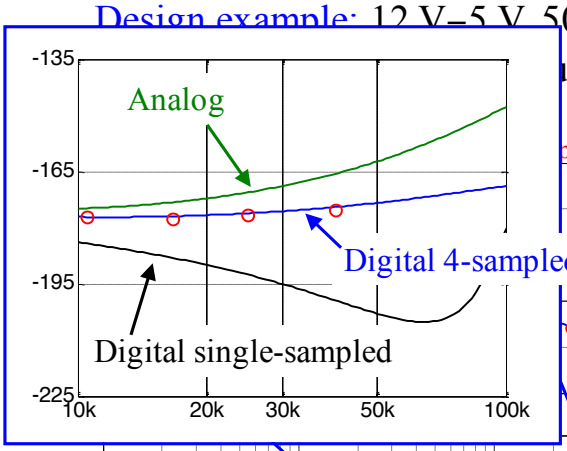
Design example: 12 V–5 V, 50 W synchronous Buck converter with triangular modulation

L=2 μH, r_L=2 mΩ, C=1 mF, ESR=1 mΩ, $f_{switching}$=200 kHz=$f_{sampling}$



Single- vs. Multi-sampled Dynamics

Design example: 12 V–5 V, 50 W synchronous Buck converter
ılar modulation



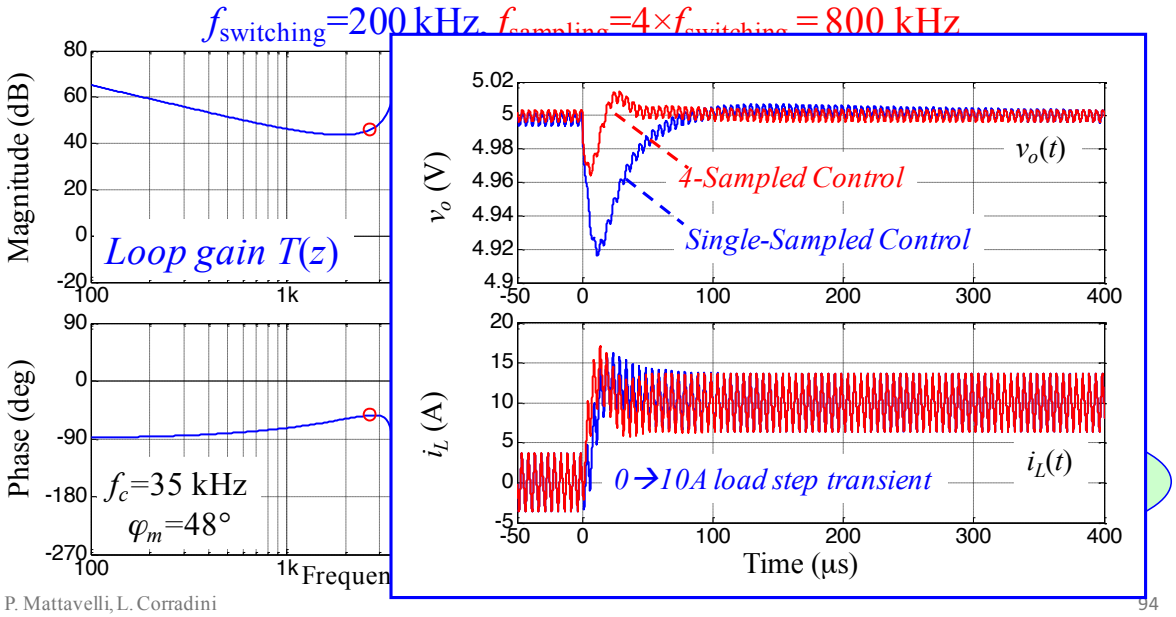
oling=4×$f_{switching}$ = 800 kHz

The increased sampling frequency reduces the PWM-related delay by a factor N

System better "approximates" analog behavior

Single- vs. Multi-sampled Dynamics

Design example: 12 V–5 V, 50 W synchronous Buck converter with triangular modulation



Summary on Small-Signal Modeling Approaches

- Two modeling techniques have been discussed:
  - I. Continuous-Time Modeling: pure *s*-domain approach. Based on averaged small-signal models used for analog control design.
    - Pros: easy to use, based on Laplace transform analysis.
    - Cons: approximate. Does not capture important sampling effects.
  - II. Discretization-Based Modeling: *z*-domain approach. Based on a specific *s*-to-*z* discretization of continuous-time models.
    - Pros:
      - Provides exact modeling for Buck-type topologies
      - Very good approximations for sampling at the middle of on/off period for current control
    - Cons: approximate for other types of topologies and/or for different sampling instant.

- An exact discrete-time small-signal modeling is possible ([11], [61]), which provides a precise approach at the expense of a mathematical complexity:

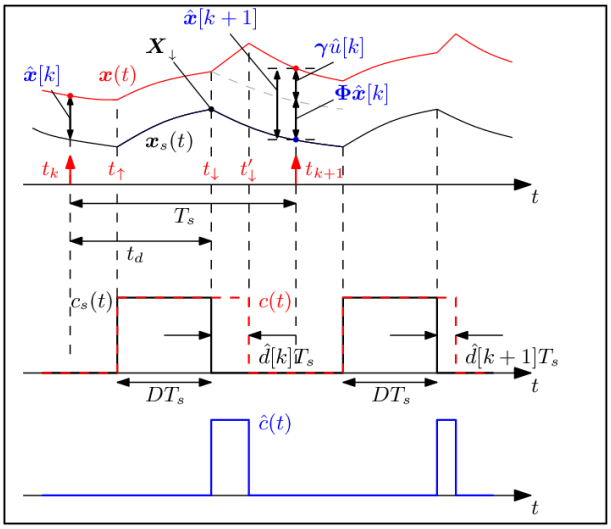
- The complete discrete-time small-signal model in state-space form is

$$\begin{cases} \hat{\mathbf{x}}[k+1] = \boldsymbol{\Phi} \cdot \hat{\mathbf{x}}[k] + \boldsymbol{\gamma} \cdot \hat{u}[k] \\ \hat{\mathbf{y}}[k] = \boldsymbol{\delta} \cdot \hat{\mathbf{x}}[k] \end{cases}$$

- In the z-domain, the input-output transfer function matrix $\mathbf{W}(z)$ is

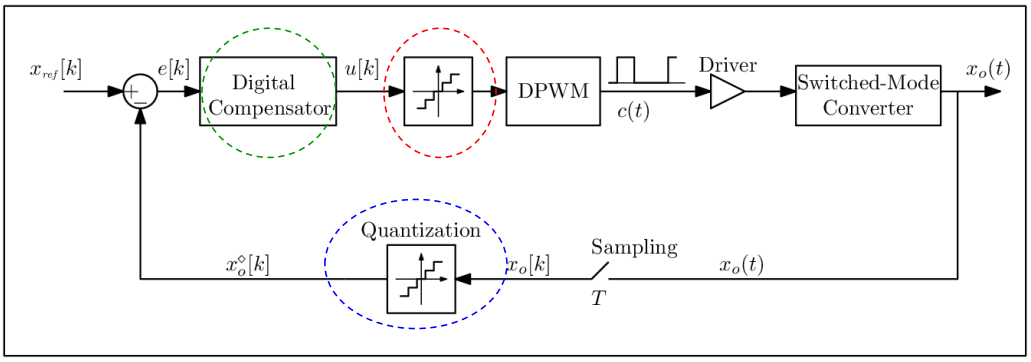
$$\mathbf{W}(z) = \frac{\hat{\mathbf{y}}(z)}{\hat{u}(z)} = \boldsymbol{\delta}\left(z\mathbf{I} - \boldsymbol{\Phi}\right)^{-1}\boldsymbol{\gamma}$$

- Entries of $\mathbf{W}(z)$ are the control-to-output small-signal transfer functions of the digitally controlled converter.



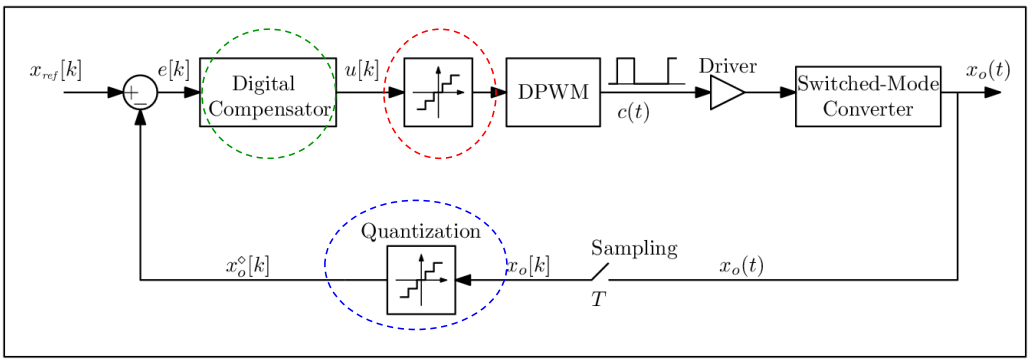
Part III
Quantization Effects

Quantizations



- The above control loop contains three quantizations:
  - Input quantization due to A/D conversion
  - Output quantization due to finite DPWM resolution
  - Control quantization due to finite precision arithmetic

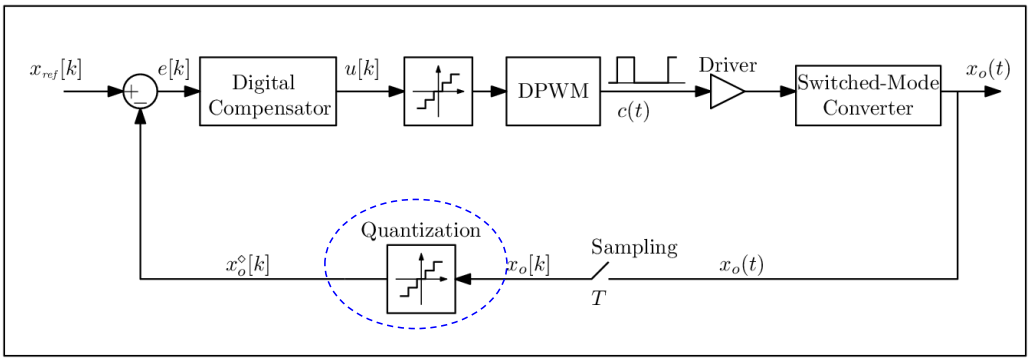
Quantizations



- The above control loop contains three quantizations:
  - Input quantization due to A/D conversion
  - Output quantization due to finite DPWM resolution
  - Control quantization due to finite precision arithmetic

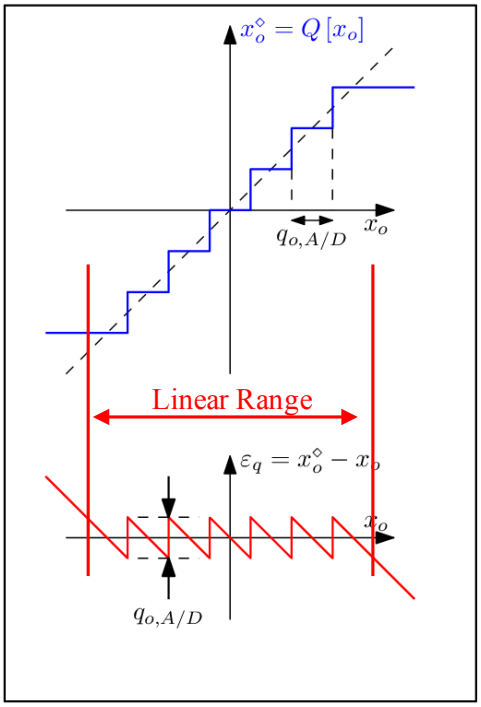
In the following, the discussion is limited to the first two types of quantization

Input Quantization



Input Quantization

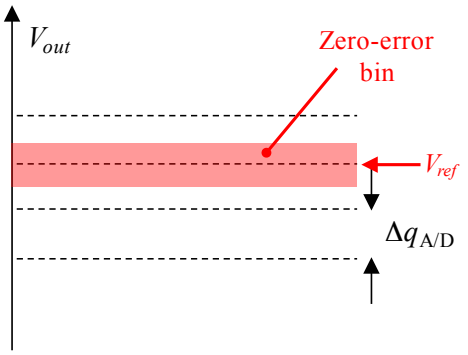
- The quantizer has a so called *linear range*, within which the quantization error remains bounded to within $|e_q| < q_{o,A/D}/2$
- Outside the linear range the quantizer saturates, and the quantization error magnitude increases as $|x_o|$ increases.
- Each input interval corresponding to the same output level is commonly called bin. Input values belonging to the same bin are *indistinguishable* to the digital compensator.



Input Quantization

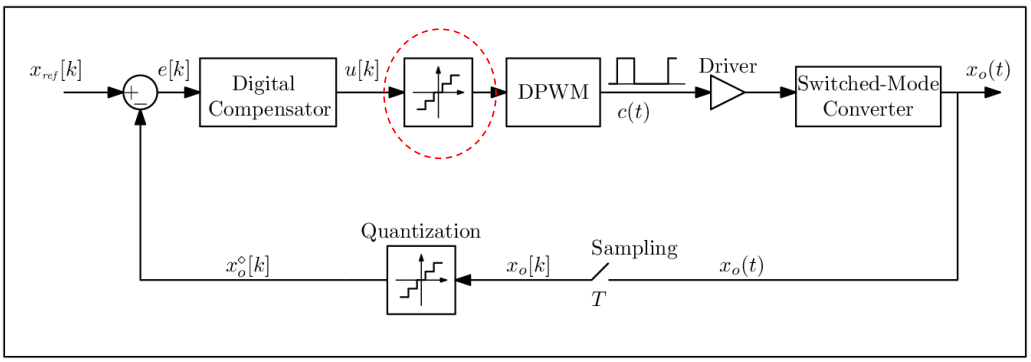
- In regulation applications, the output signal x_o can therefore only be regulated to within $\pm q_{o,A/D}/2$.
- The *zero error bin* is the bin inside which it is desired to regulate the output. It is identified by a digital setpoint X_{ref}.
- Note that when the sampled output lies inside the zero error bin, the control error e is zero*:

$$e = X_{ref} - x_{o,q} = 0.$$



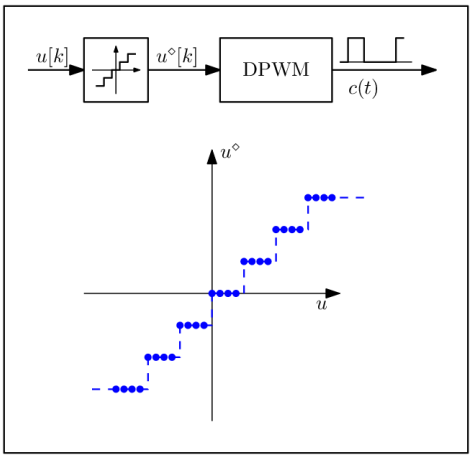
* Do not confuse the quantization error e_q with the control error e!

Output Quantization



Output Quantization

- The digital compensator is typically capable of calculating the control command $u[k]$ with a resolution much higher than what the modulator is capable of. For such reason, $u[k]$ is quantized into a lower resolution signal $u^{\Diamond}[k]$ before being acquired by the DPWM.
- Such quantization can be modeled as a process in which some of the least significant bits of u are eliminated via either *round-off* or *truncation*.
- The Figure represents the $u^{\Diamond}$ vs. u quantization characteristic when the two least significant bits of u are truncated.

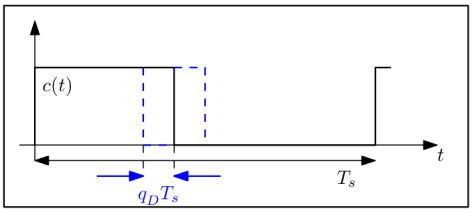


Output Quantization

- Quantization of u corresponds to the minimum duty cycle variation q_D the modulator can generate.
- In turn, q_D induces a corresponding quantization $q_{o,DPWM}$ of the output voltage range.
- In the case of Buck converter: $V_{out} = D \cdot V_g \quad \Rightarrow \quad q_{o,DPWM} = q_D \cdot V_g$
- More generally, if $M(D)$ is the converter conversion ratio:

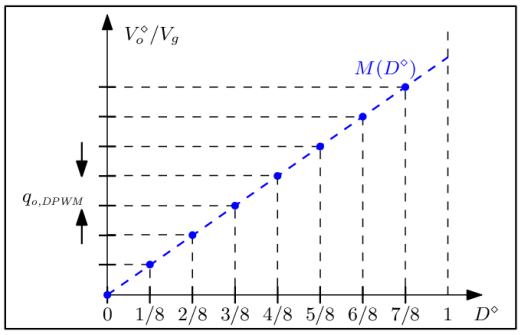
$$V_{out} = M(D) \cdot V_g$$
$$\Rightarrow \quad q_{o,DPWM}(D) \cong \frac{\partial M}{\partial D} \cdot q_D \cdot V_g$$

- Observe that, in general, $q_{o,DPWM}$ depends upon the converter operating point.

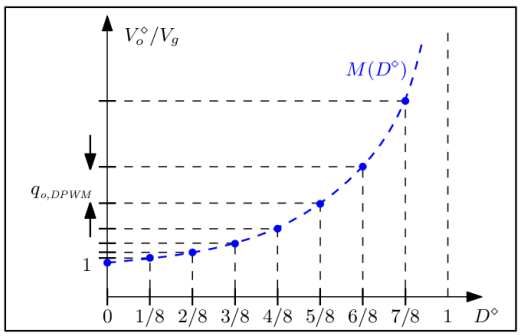


Output Quantization: Examples

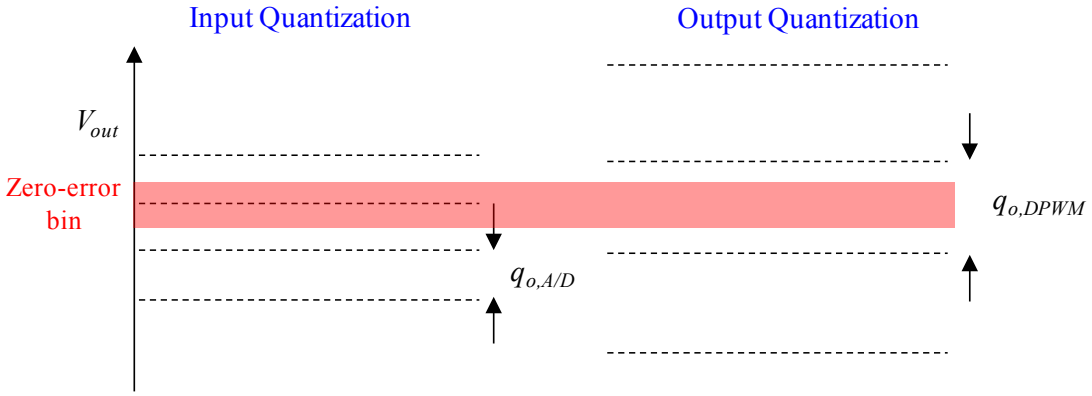
- Buck converter example:
  - $q_{o,DPWM} = q_D V_g$
  - Quantization on V_o is *uniform* as long as V_g is fixed



- Boost converter example:
  - $q_{o,DPWM} \approx q_D V_g/(1-D)^2$
  - Quantization on V_o depends on the operating point D even with V_g fixed.

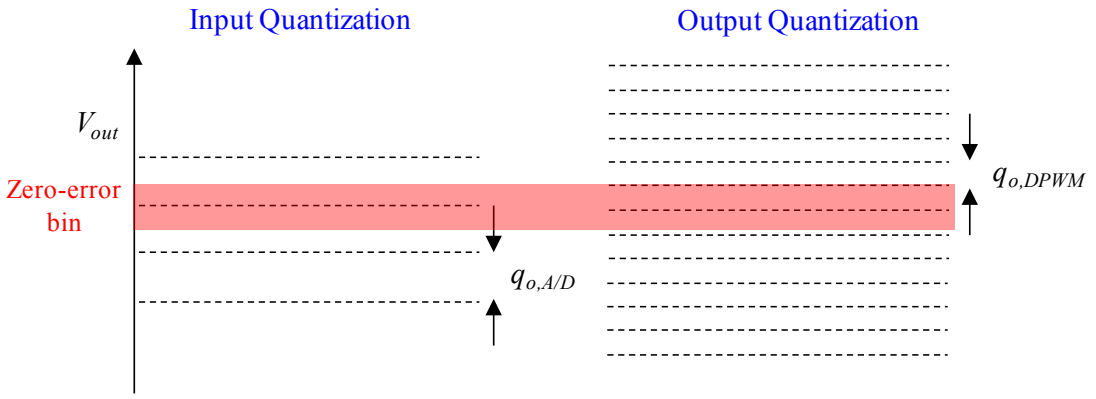


Interaction Between Input and Output Quantizations



- If no output quantization level falls within the zero error bin, the digital controller will never reach a steady-state condition.
- As a result, a permanent oscillation arises, in which the output voltage endlessly moves around the zero error bin.
- Such oscillation, inherently nonlinear in nature, is an example of limit cycle.

Interaction Between Input and Output Quantizations



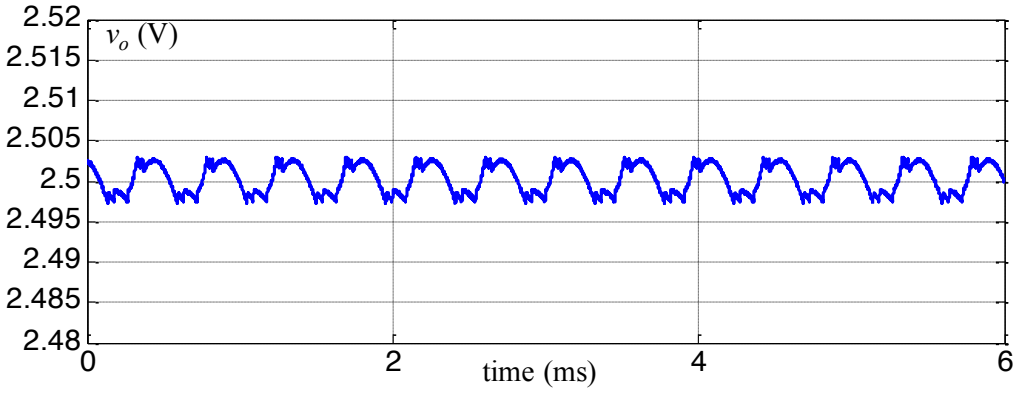
- In order to prevent the above condition to occur, the DPWM resolution – expressed in terms of output voltage – needs to be finer than the A/D resolution:

$$q_{o,DPWM} < q_{o,A/D}$$

(No-limit-cycling condition #1)

- Such condition, however, is necessary but **not** sufficient to prevent limit cycling.

Example of Limit Cycle

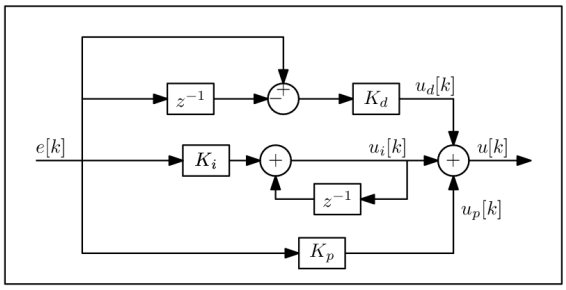


- In the example, $q_{o,DPWM} > q_{o,A/D}$
- ➔ A low-frequency limit cycle arises

Effect of the Integral Gain

- Consider now a digital PID compensator such as the one reported in the Figure. Suppose the sensing gain of the feedback is unity, i.e. H=1.
- Assume also the system to be ***in steady-state and with no limit cycles***. Since the feedback contains one integrator, it follows that $e[k]$=0.
- This means that both the proportional and derivative components of the control signal are zero, while the integral term is constant:

$$u[k] = u_i[k] = \text{constant}$$



Effect of the Integral Gain

- The integral term can be written as

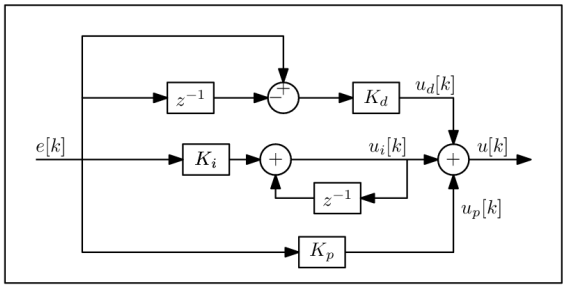
$$u_i[k] = K_i \cdot \sum_{n=-\infty}^{k} e[n]$$

- Since $e[k]$ is a digital sequence, each $e[n]$ is an **integer** multiple $l[n]$ of the A/D quantization step $q_{o,A/D}$:

$$u_i[k] = K_i \cdot q_{o,A/D} \cdot \sum_{n=-\infty}^{k} l[n]$$

- Since $u[k] = u_i[k] =$ constant, the summation of the $l[n]$ terms must converge to some integer N:

$$u[k] = K_i \cdot q_{o,A/D} \cdot N$$

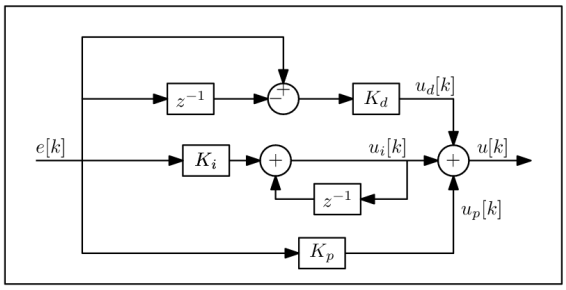


Effect of the Integral Gain

- Equation

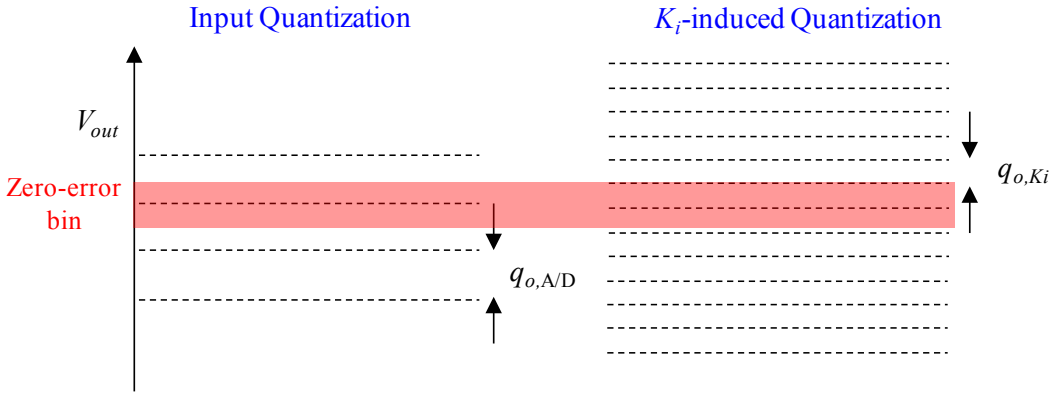
$$u[k] = K_i \cdot q_{o,A/D} \cdot N$$

implies that, in steady-state, $u[k]$ is quantized by $K_i \cdot q_{o,A/D}$. In other words, $u[k]$ inherits the granularity of $e[k]$, scaled by the integral gain K_i.



- Similarly to what seen in regard to the DPWM quantization, one must therefore expect such quantization to induce a corresponding granularity $q_{o,Ki}$ on the output voltage.

Effect of the Integral Gain



- Given the initial assumption of steady-state operation with no limit cycles, it **necessarily** follows that at least one K_i quantization level falls inside the zero-error bin:

$$q_{o,Ki} < q_{o,A/D} \quad \Rightarrow \quad \frac{1}{N_r} G_{vd}(s=0) \cdot H \cdot K_i < 1$$

(No-limit-cycling condition #2)

Comments

- No-limit-cycling conditions #1 and #2

$$q_{o,DPWM} < q_{o,A/D} \qquad \frac{1}{N_r} G_{vd}(s=0) \cdot H \cdot K_i < 1$$

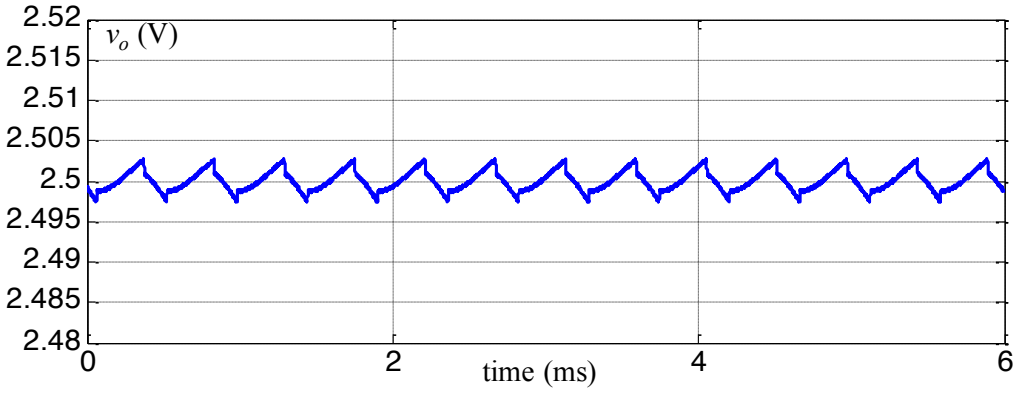
can be regarded as *necessary, but not sufficient* to guarantee absence of limit cycles.

- From a design standpoint, the above equations nonetheless serve as good starting points. Further investigations on the possible occurrence of limit cycle oscillations are best performed via simulation.
- In the case of voltage-mode control of a Buck converter one has $G_{vd}(0) = V_g$, and the second condition becomes

$$\frac{1}{N_r} V_g \cdot H \cdot K_i < 1$$

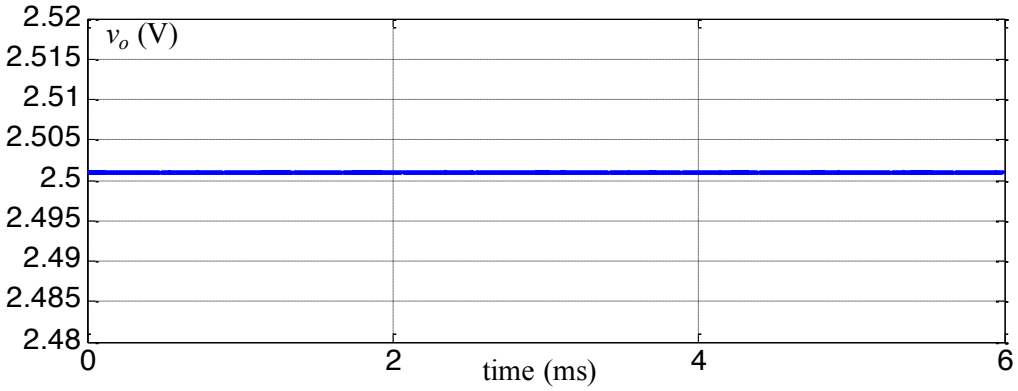
Large V_g's tend to make $q_{o,Ki}$ larger, potentially triggering limit cycle oscillations.

Effect of the Integral Gain: Example



- In the previous example, $q_{o,DPWM}$ is reduced so as to satisfy $q_{o,DPWM} < q_{o,A/D}$.
- The limit cycle, however, persists. The reason is that the controller integral gain violates the no-limit cycle condition.

Effect of the Integral Gain: Example



- After the integral gain is reduced, the limit cycle vanishes.

Bibliography

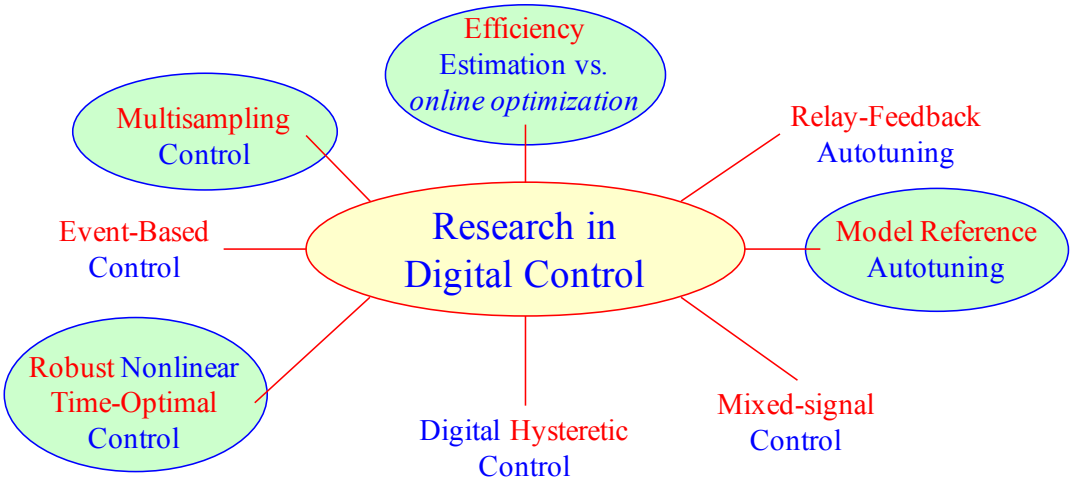
- No-limit-cycling conditions presented here have been originally discussed in [43]:
  - A. Peterchev, S. Sanders, "Quantization Resolution and Limit Cycling in Digitally Controlled PWM Converters," *IEEE Trans. Power Electron.*, Vol. 18, No. 1, pp. 303-318, Jan. 2003.
- Further no-limit-cycling conditions are formulated in [46]:
  - H. Peng, A. Prodić, E. Alarcón, D. Maksimović, "Modeling of Quantization Effects in Digitally Controlled DC-DC Converters," *IEEE Trans. Power Electron.*, Vol. 22, No. 1, pp., 208-215, Jan. 2007
- For an additional discussion on finite precision arithmetic effects, see [61]:
  - L. Corradini, D. Maksimović, P. Mattavelli and R. Zane, "Digital Control of High-Frequency Switched-Mode Power Converters," 1st ed. Wiley-IEEE Press, Jul. 2015

Part IV
Advances in Digital Control for High-Frequency dc-dc Converters

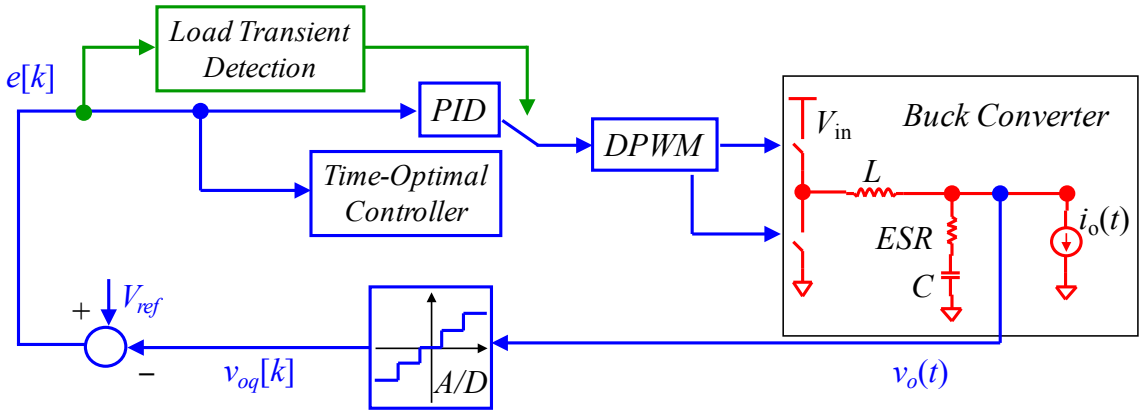
Research in Digital Control of High-Frequency Power Converters

Focus on high-performance, low hardware complexity control solutions capable to:

1. Be competitive against well-established analog controllers
2. Offer new features, not available with analog ICs



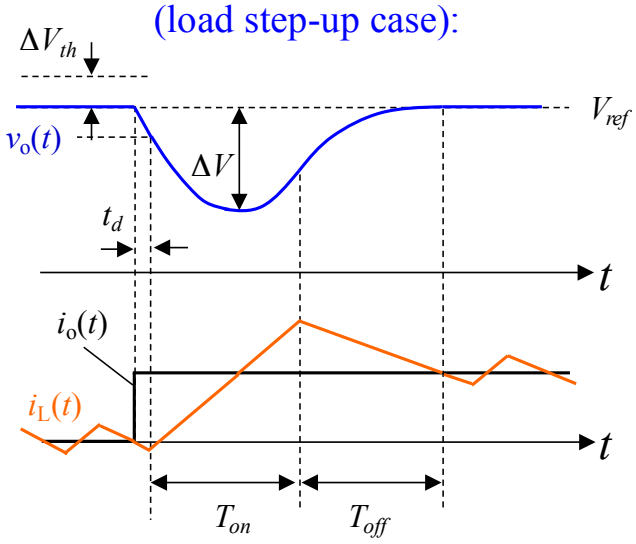
Digital Time-Optimal Control



- A conventional PID controller is active during normal operation
- A nonlinear time-optimal controller (TOC) takes over when a load change is detected
- The TOC control recovers the voltage error with a single on/off switching action

Digital Time-Optimal Control

Time-Optimal Transient (load step-up case):

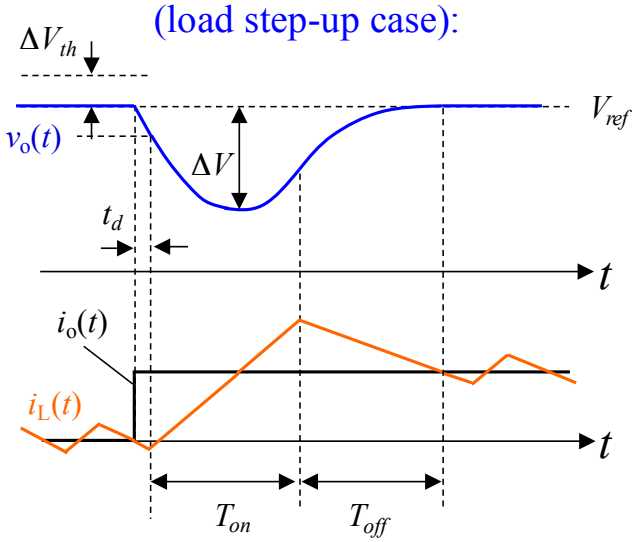


Once the load change is detected:

1. Primary switch is turned on for a time interval T_{on}
2. Primary switch is turned off (and synchronous switch is turned on) for a time interval T_{off}
3. If T_{on} and T_{off} are properly timed, the output voltage is brought back to regulation *in minimum time*

Digital Time-Optimal Control

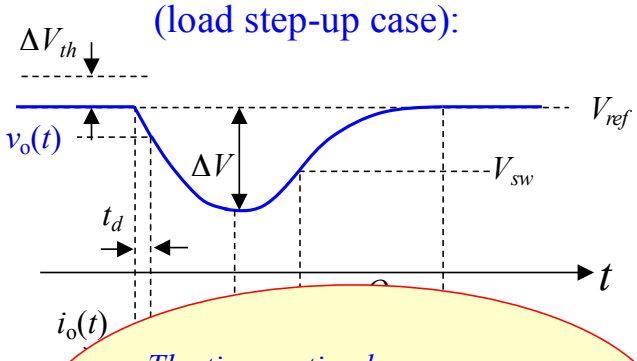
Time-Optimal Transient (load step-up case):



- Both T_{on} and T_{off} depend on the power stage parameters.
- However, *it is possible* to realize a Time-Optimal switching sequence without preliminary knowledge of the power stage parameters, *as long as times and voltages can be measured "on the fly"* ***during the transient***.

Parameter-Independent Time-Optimal Control

Time-Optimal Transient (load step-up case):



The time-optimal sequence can be implemented robustly as long as T_2 and ΔV can be measured on the fly during the transient

independent time-optimal equations

Principles involved (assume t_d=0):

$$Q_1 + Q_{23} = 0$$

Charge balance, **does not depend on *C***

$$i_L(T_1) = i_L(T_1 + T_2 + T_3)$$

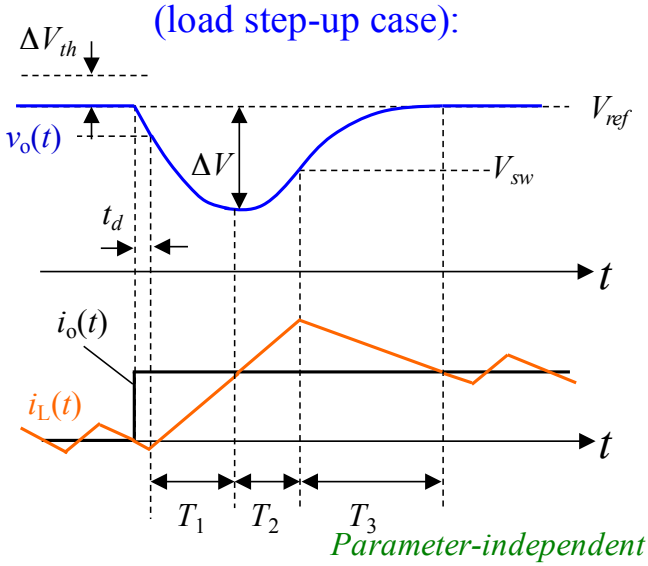
Volt-second balance, **does not depend on *L***

$$T_3 = \frac{1-D}{D} T_2$$

$$V_{sw} = V_{ref} - (1-D)\Delta V$$

Parameter-Independent Time-Optimal Control

Time-Optimal Transient (load step-up case):



Parameter-independent time-optimal equations

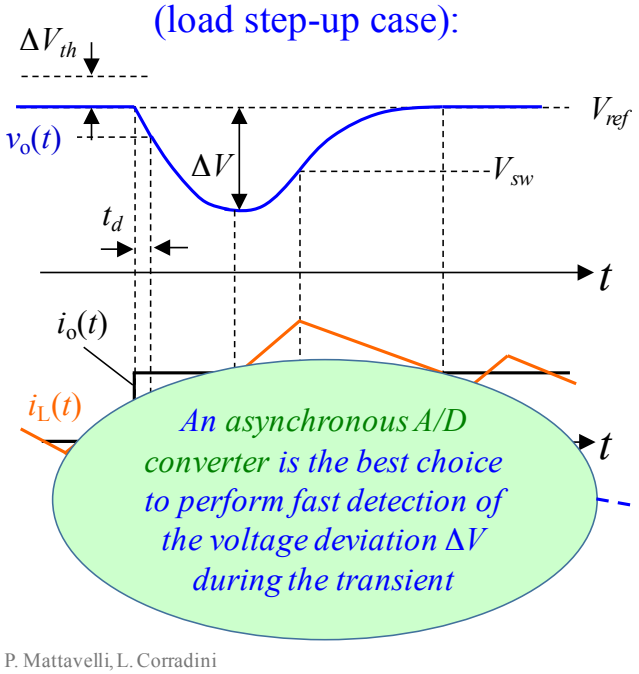
$$T_3 = \frac{1-D}{D} T_2$$
$$V_{sw} = V_{ref} - (1-D)\Delta V$$

Robust time-optimal sequence:

1. Upon transient detection, turn primary switch on
2. At the valley point, measure the value of output voltage deviation ΔV and calculate V_{sw}
3. Measure time interval T_2 as $v_o(t)$ reaches V_{sw}
4. At $v_o(t)=V_{sw}$, turn switch off and calculate T_3
5. At the end of T_3, return to PID operation

Parameter-Independent Time-Optimal Control

Time-Optimal Transient (load step-up case):



An asynchronous A/D converter is the best choice to perform fast detection of the voltage deviation ΔV during the transient

$$T_3 = \frac{1-D}{D} T_2$$
$$V_{sw} = V_{ref} - (1-D)\Delta V$$

Robust time-optimal sequence:

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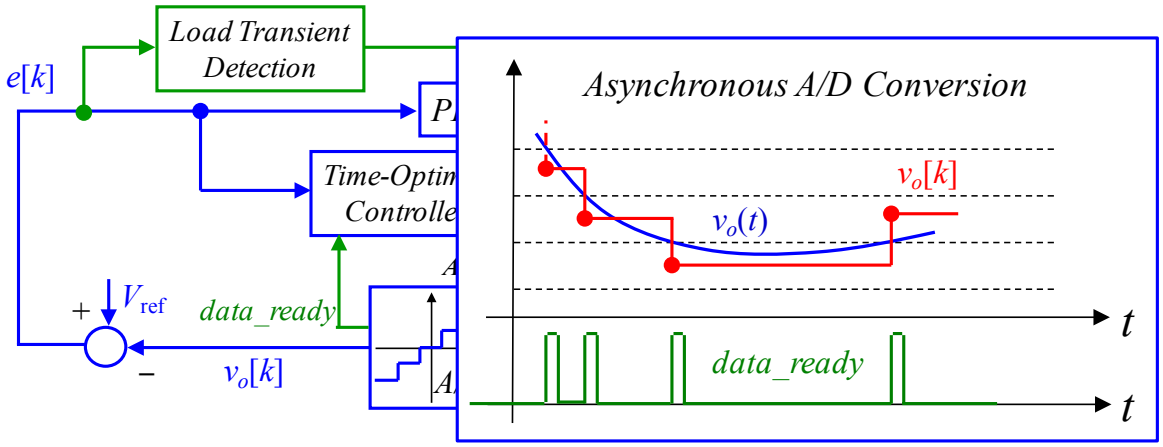
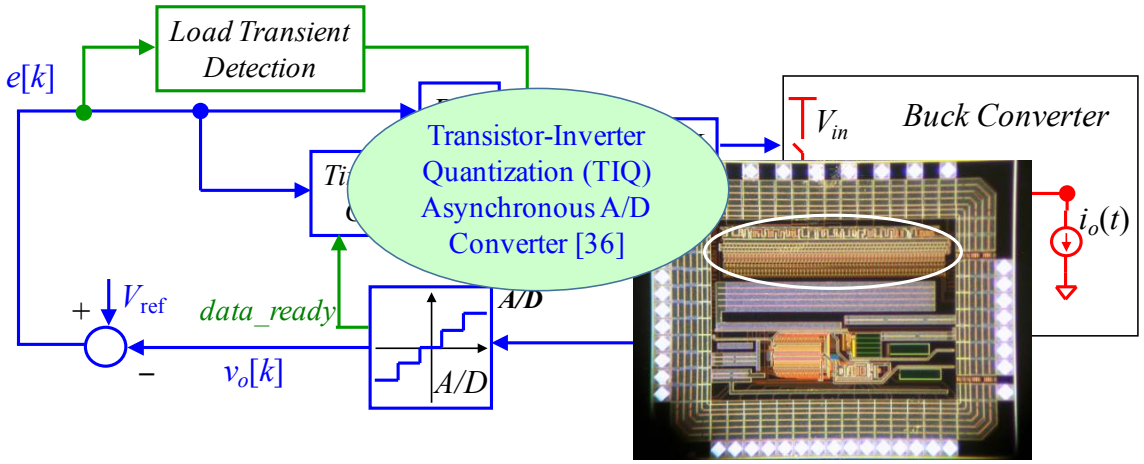
5. At the end of T_3, return to PID operation

Asynchronous A/D Sampling



- An asynchronous A/D converter quantizes the output voltage as soon as it crosses a quantization level
- A *data_ready* flag is asserted upon every conversion
- Viable approach for fast acquisition during the Time-Optimal Transient

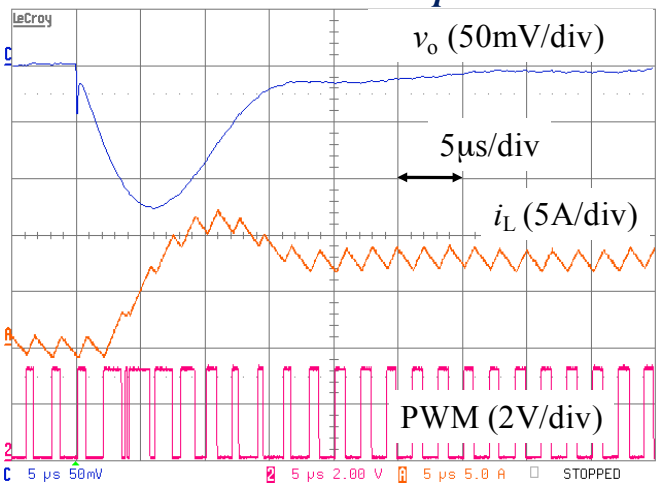
Asynchronous A/D Sampling



- An asynchronous A/D converter quantizes the output voltage as soon as it crosses a quantization level
- A *data_ready* flag is asserted upon every conversion
- Viable approach for fast acquisition during the Time-Optimal Transient

Experimental Results: Conventional PID Control

0–8A load step response
Conventional PID Compensation



PID Design:
f_c=43 kHz, φ_m=43°

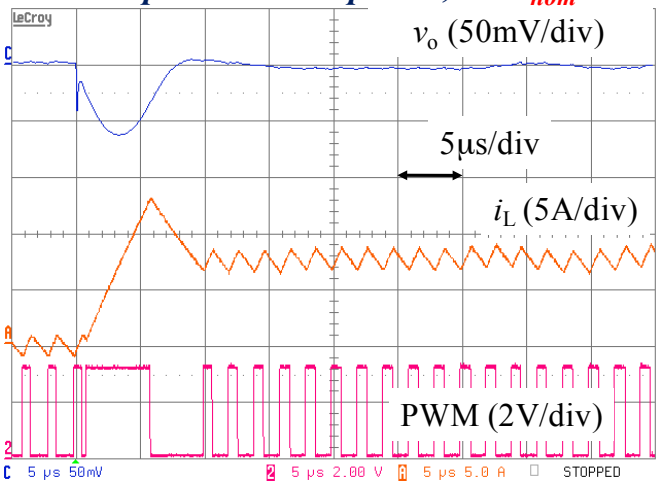
Experimental case study:

- 5 V – 1.6 V synchronous buck, f_s=500 kHz, L=1.1 µH, C_{nom}=250 µF (ceramic)
- Asynchronous A/D quantization step Δq=3 mV
- Load detection threshold ΔV_{th}=12 mV

- Experimental tests:
  - Conventional PID
  - Proposed Time-Optimal, Voltage Based Approach
  - Tests for different values of the output capacitance

Experimental Results: Time-Optimal Control

0–8A load step response
Proposed Time-Optimal, $C=C_{nom}$



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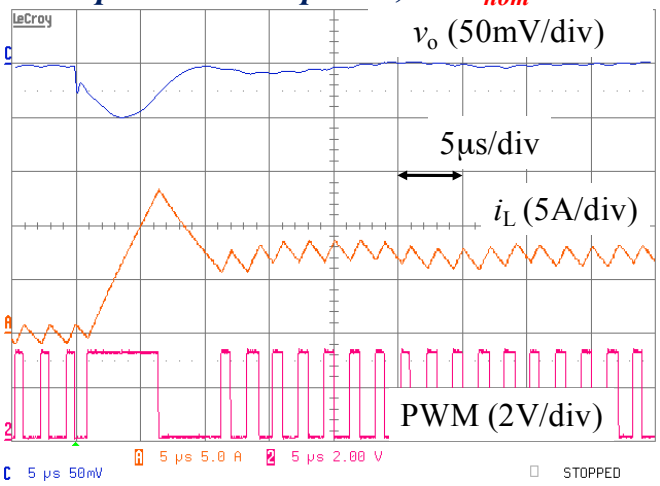
Experimental Results: Time-Optimal Control

0–8A load step response
Proposed Time-Optimal, $C=C_{nom}$+56%



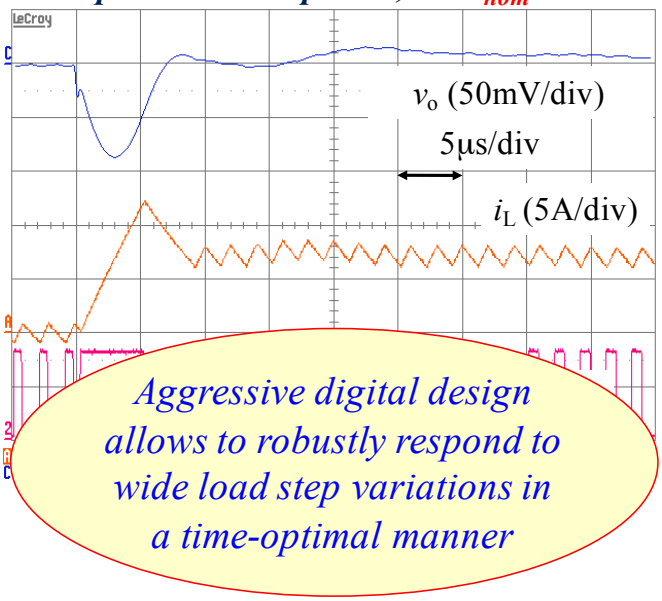
Experimental case study:

- 5 V – 1.6 V synchronous buck, f_s=500 kHz, L=1.1 µH, C_{nom}=250 µF (ceramic)
- Asynchronous A/D quantization step Δq=3 mV
- Load detection threshold ΔV_{th}=12 mV

- Experimental tests:
  - Conventional PID
  - Proposed Time-Optimal, Voltage Based Approach
  - Tests for different values of the output capacitance

Experimental Results: Time-Optimal Control

0–8A load step response
Proposed Time-Optimal, $C=C_{nom}$–40%



Aggressive digital design allows to robustly respond to wide load step variations in a time-optimal manner

Experimental case study:

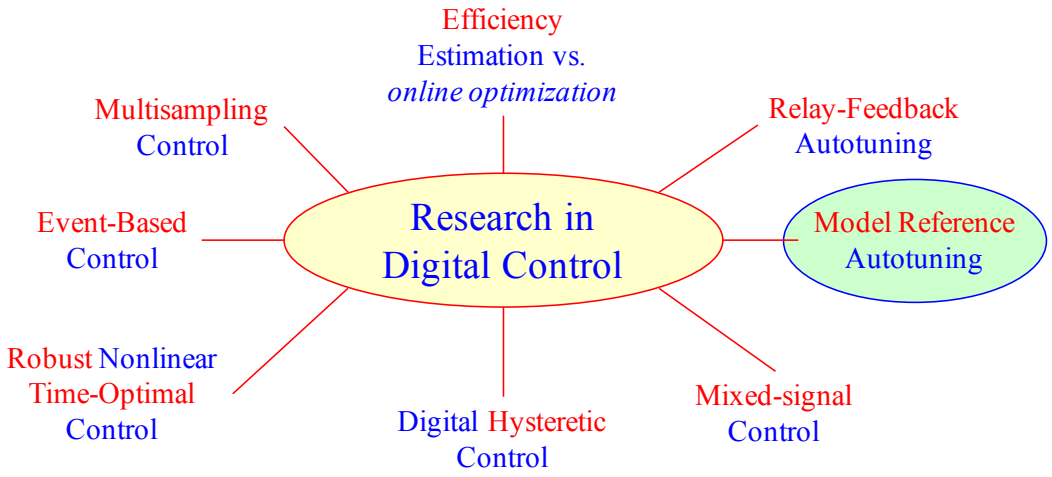
- 5 V – 1.6 V synchronous buck, f_s=500 kHz, L=1.1 µH, C_{nom}=250 µF (ceramic)
- Asynchronous A/D quantization step Δq=3 mV
- Load detection threshold ΔV_{th}=12 mV

- Experimental tests:
  - Conventional PID
  - Proposed Time-Optimal, Voltage Based Approach
  - Tests for different values of the output capacitance

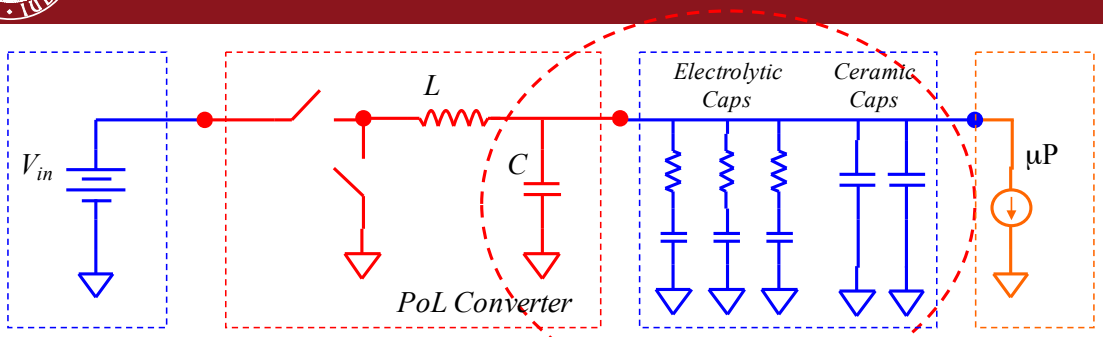
Research in Digital Control of High-Frequency Power Converters

Focus on high-performance, low hardware complexity control solutions capable to:

1. Be competitive against well-established analog controllers
2. Offer new features, not available with analog ICs



Digital Autotuning

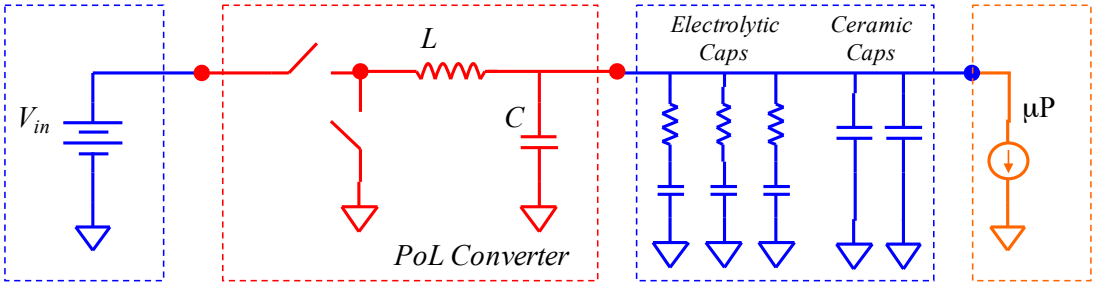


Design challenges in Point-of-Load converters:

- Number, types and values of load decoupling capacitors often unknown to the designer
- Component tolerances
- Temperature variations or aging

Equivalent capacitance and ESR may vary over orders of magnitude

Digital Autotuning



Control design approaches

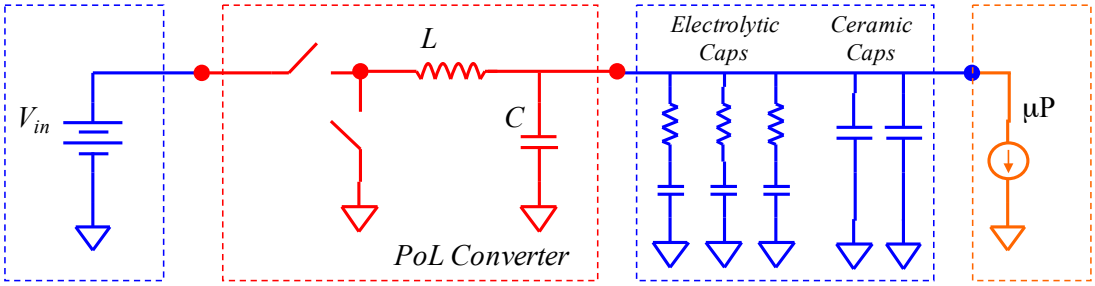
Standard, worst case design:

- Must accept significant penalties in closed loop performances
- Unable to track process parametric variations

Self-tuning digital controllers:

- *Optimized* closed loop bandwidth while maintaining proper stability margins
- *Online tuning* is possible to track process variations

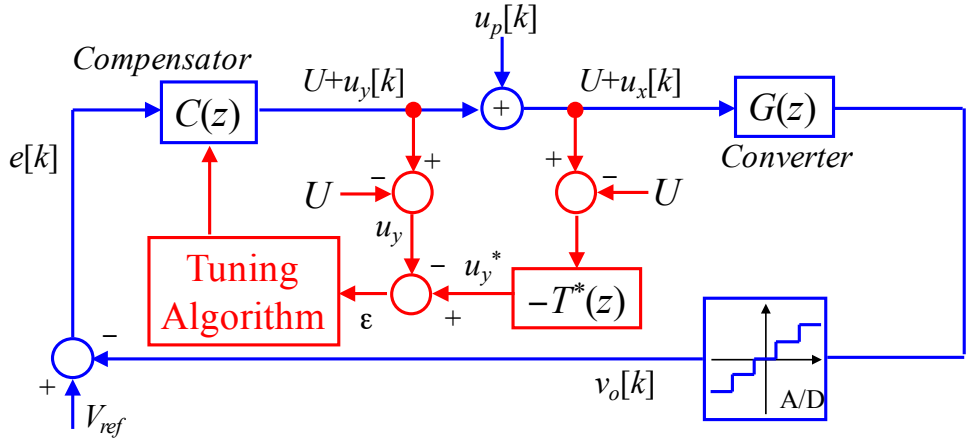
Digital Autotuning



Objectives of the tuning algorithm

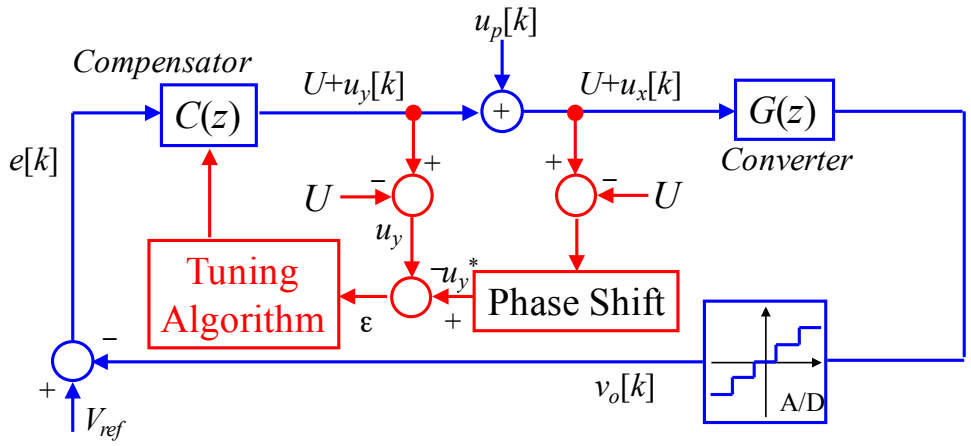
- Determine the compensator parameters in order to meet proper stability margins, and ensure adequate dynamic performances.
- Typically:
  - Phase margin $\varphi_m = \varphi_m{}^*$
  - Loop gain crossover frequency $f_c = f_c^*$

Closed-loop Autotuning based on Model Reference



- In closed-loop configuration, an input perturbation $u_p[k]$ is superimposed to the modulating signal
- The model reference expresses the desired system loop gain: $T^*(z) = C^*(z)G^*(z)$

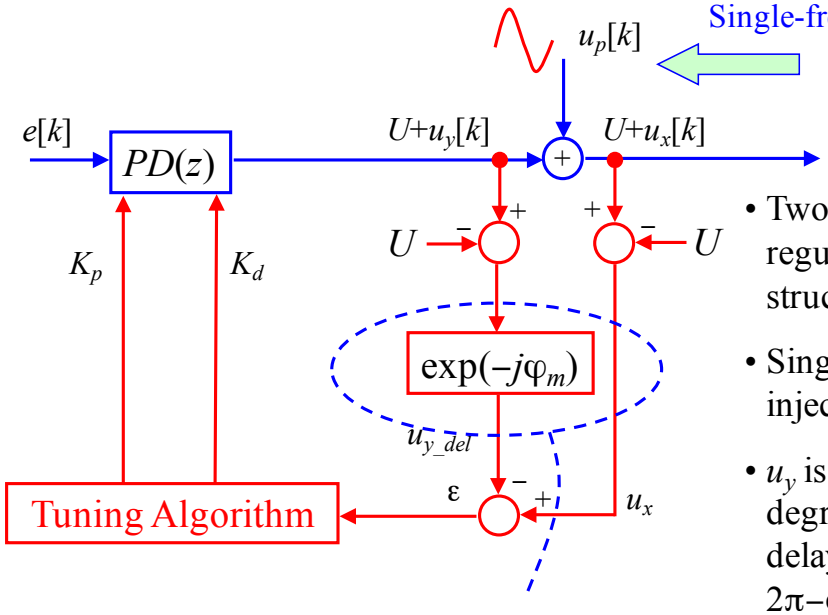
Closed-loop Autotuning based on Model Reference



- Rather than forcing condition $T(z) = T^*(z)$ at every frequency, it is imposed only at the desired crossover frequency f_c. Therefore, the model reference reduces to a simple phase shift:

$$T^*(f_c) = e^{-j(\pi-\varphi_m)} = -e^{j\varphi_m}$$

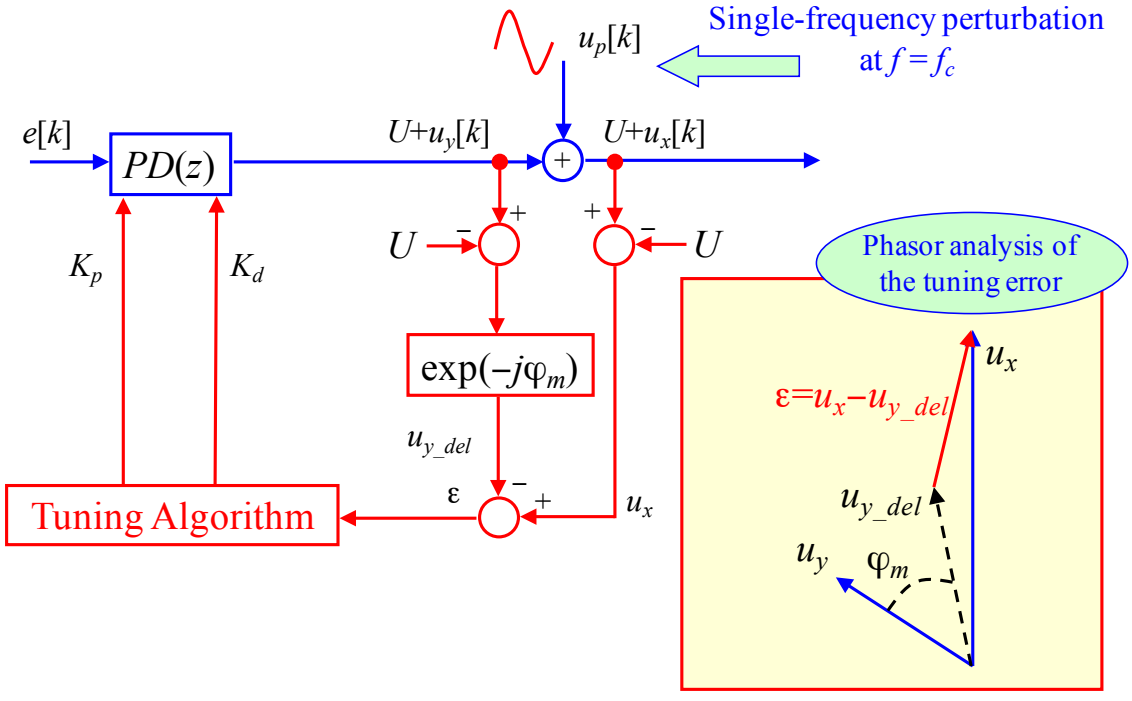
Application to Two-Parameters Regulators (PD or PI)



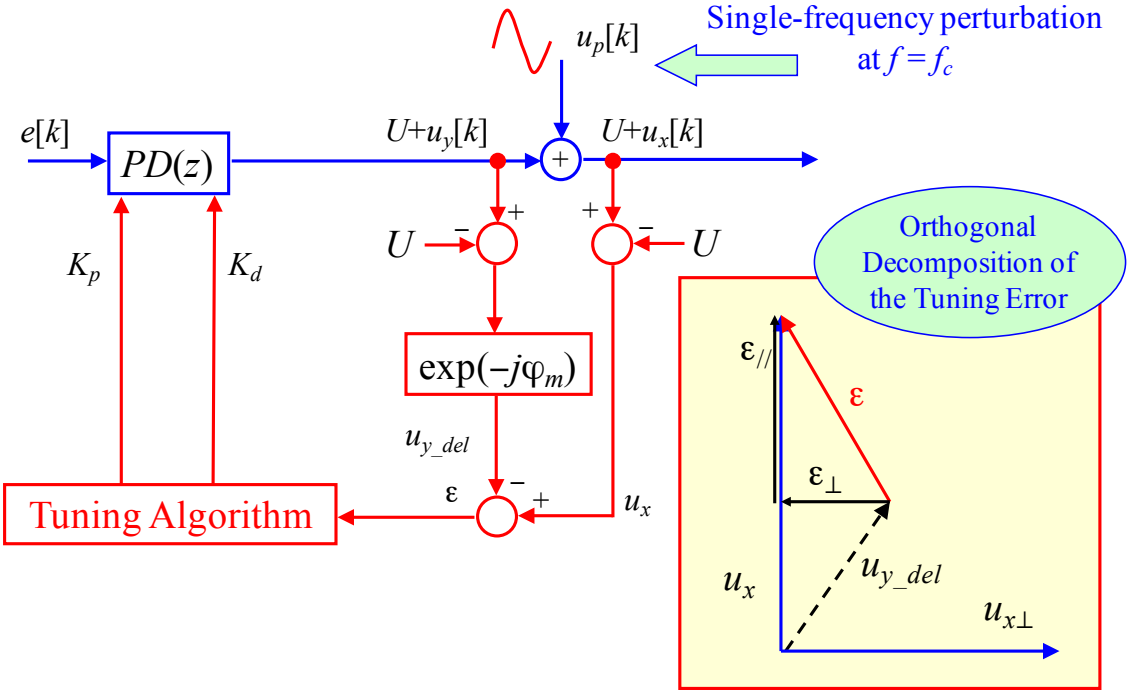
- Two-parameters regulators like PD or PI structures
- Single frequency injection
- u_y is delayed by φ_m degrees rather than delaying u_x by $2\pi-\varphi_m$
  ➔ shorter delay line

Can be implemented with z^{-N} or by means of a dedicated filter

Application to Two-Parameters Regulators (PD or PI)



Application to Two-Parameters Regulators (PD or PI)



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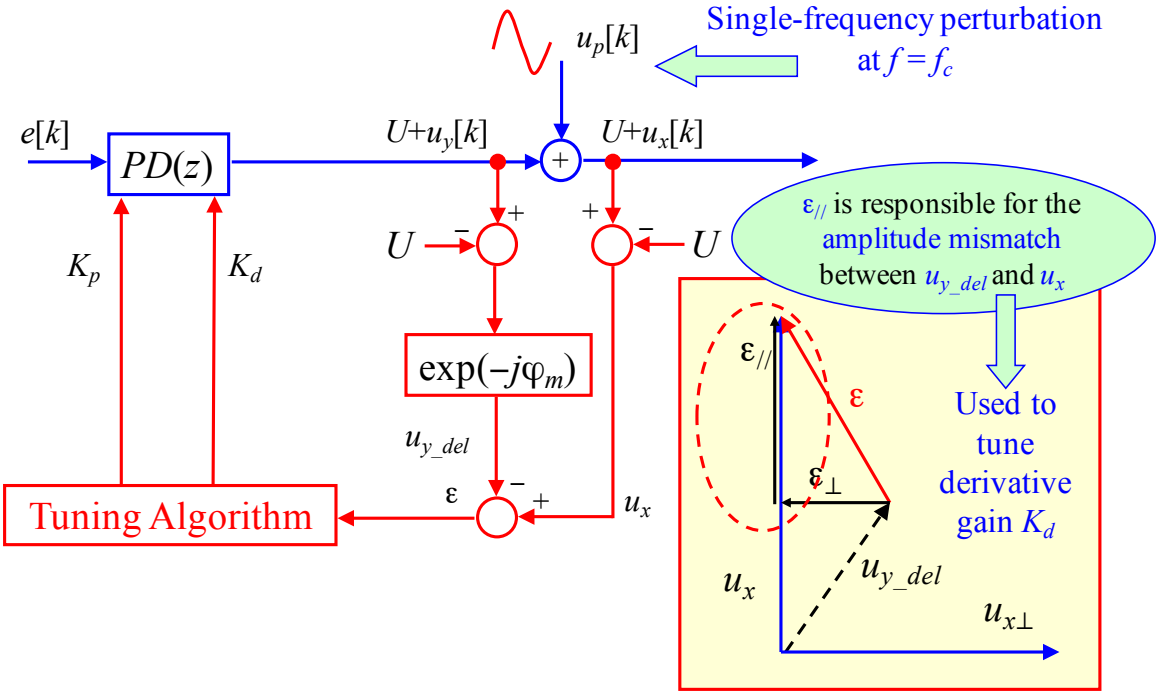
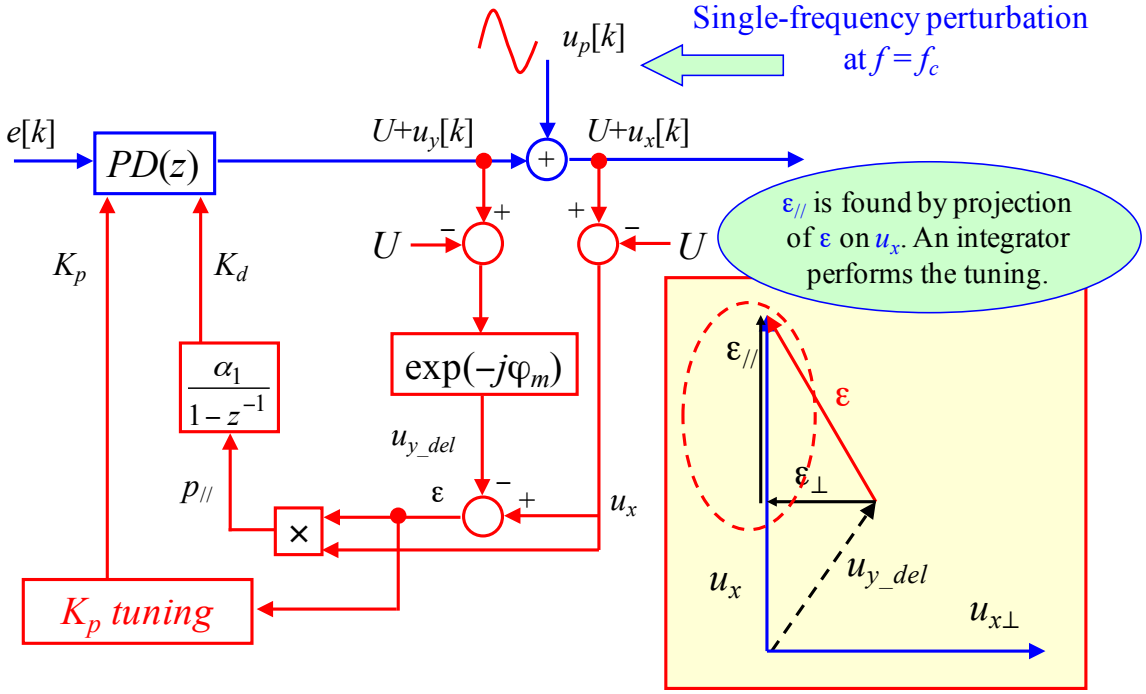
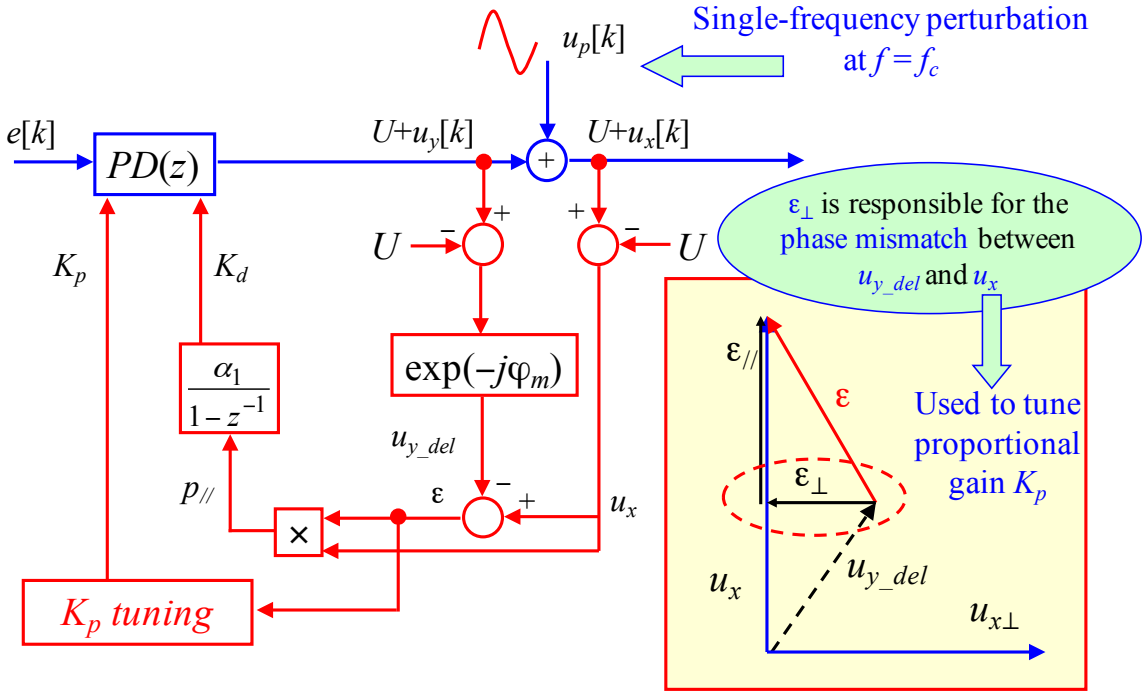


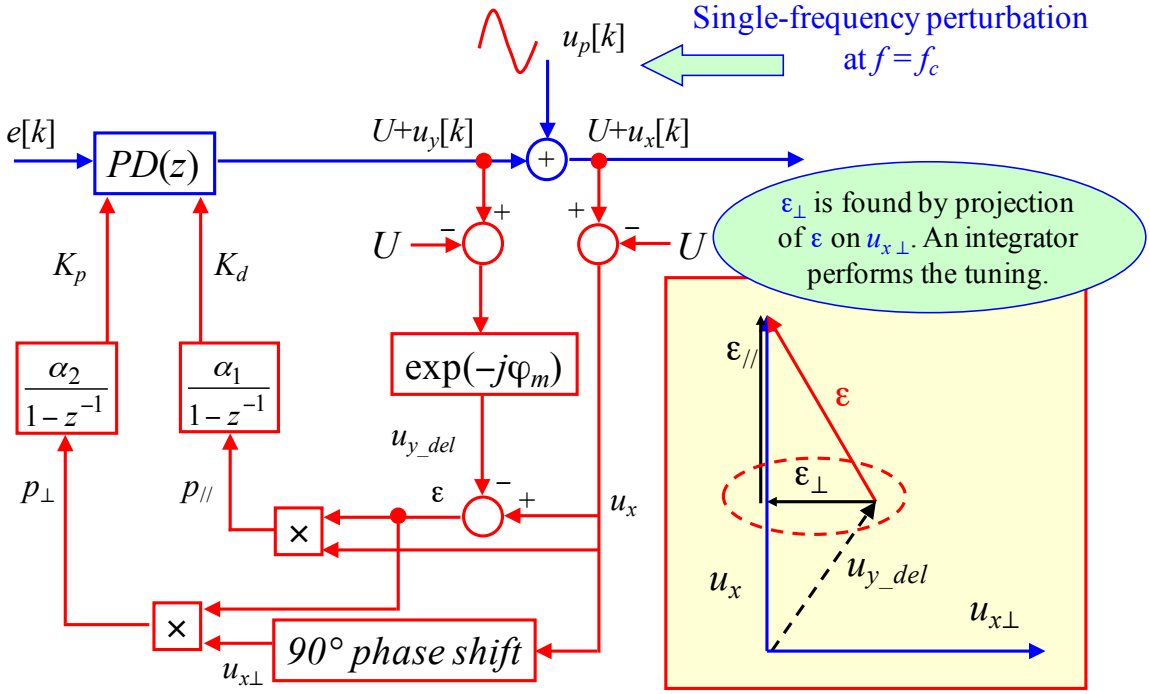
Application to Two-Parameters Regulators (PD or PI)



Application to Two-Parameters Regulators (PD or PI)

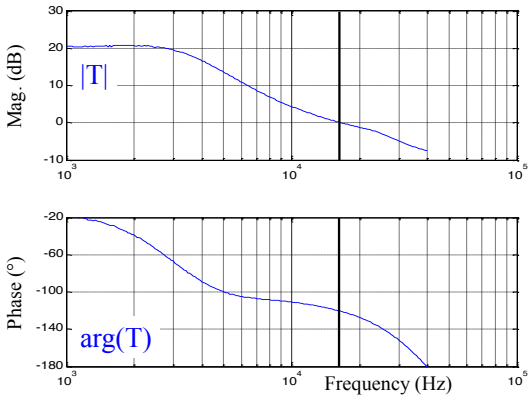


Application to Two-Parameters Regulators (PD or PI)



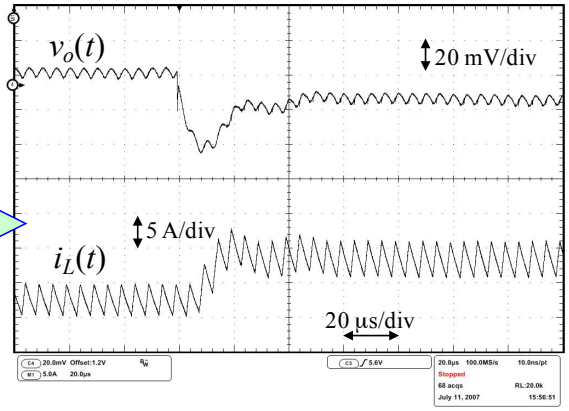
Experimental Example

Post-tuning loop gain

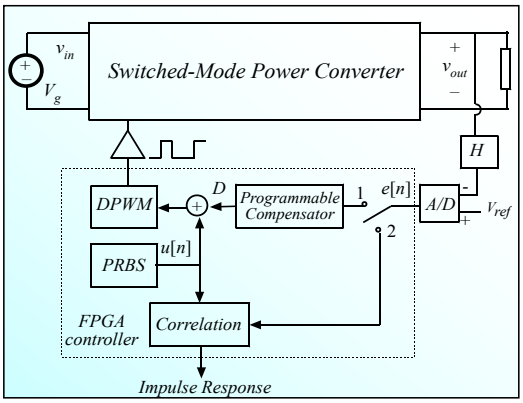


- 5 V – 1.3 V synchronous buck, f_s=200 kHz, L=800 µH, C=2.6 mF
- PD tuning
- Tuning targets: $f_c = f_s/12$, $\varphi_m = 60°$

Post-tuning 0–6 A step load response (PD compensation)



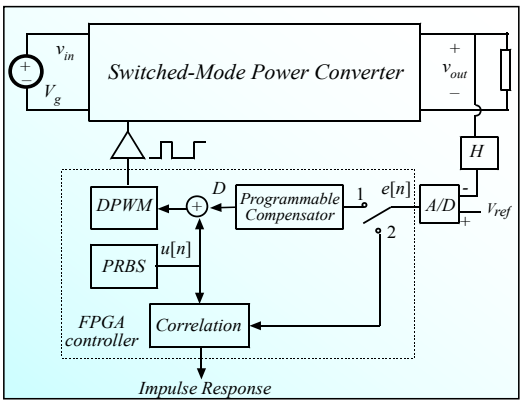
Cross-Correlation Based Identification



Reference work:

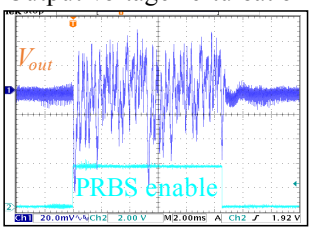
[48] B. Miao, R. Zane, D. Maksimovic, "System Identification of Power Converters with Digital Control through Cross-Correlation Methods", IEEE Transactions on Power Electronics, Vol. 20, no. 5, Sept. 2005

Cross-Correlation Based Identification



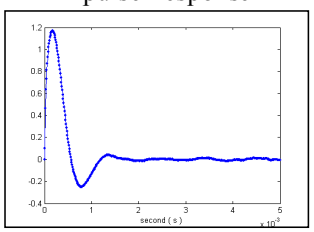
1. Inject pseudo-random binary sequence (PRBS): $d = D + u$
2. Collect output voltage perturbations
3. Cross-correlate input u with output e to get impulse response
4. Fast Fourier Transform to get frequency response

Output Voltage Perturbation



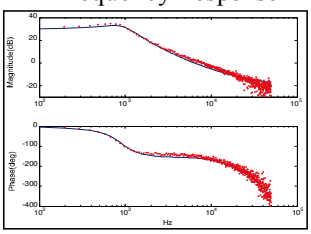
Cross-correlate

Impulse Response



FFT

Frequency Response



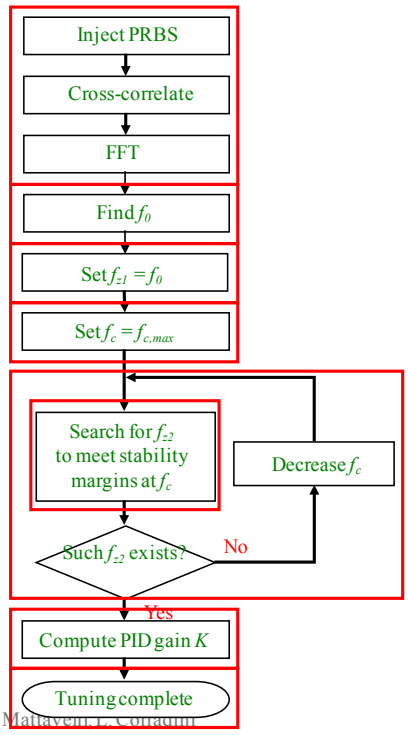
Identification Approches

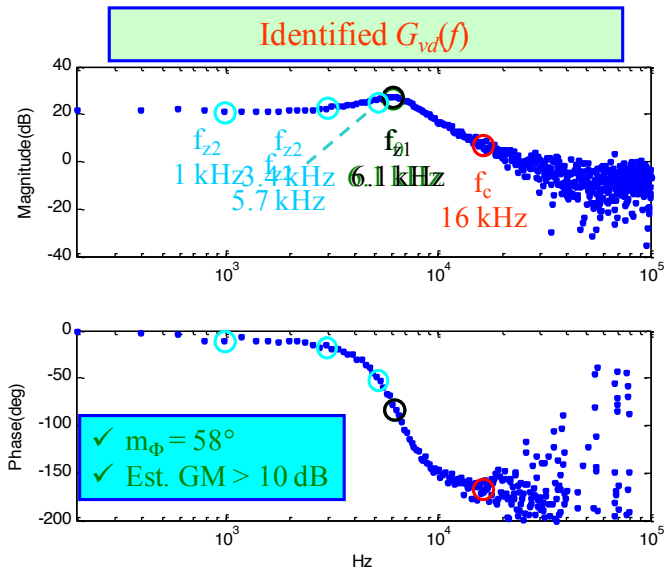
- Parametric identification: a set of parameters is estimated to best-fit the identified response with an analytical model, as in:
  - B. Miao, R. Zane, D. Maksimovic, "Automated Controller Design for Switching Converters", IEEE PESC 2005
  - ➔Accurate
  - ➔Computationally Intensive!

- Non-parametric identification: the tuning algorithm directly works on the magnitude/phase vector of the process transfer function, as in:
  - [52] M. Shirazi, L. Corradini, R. Zane, P. Mattavelli, D. Maksimovic, "Autotuning Techniques for Digitally Controlled Point-of-Load Converters with Wide Range of Capacitive Loads", IEEE APEC 2007

"System-ID Autotuning" (CoPEC)

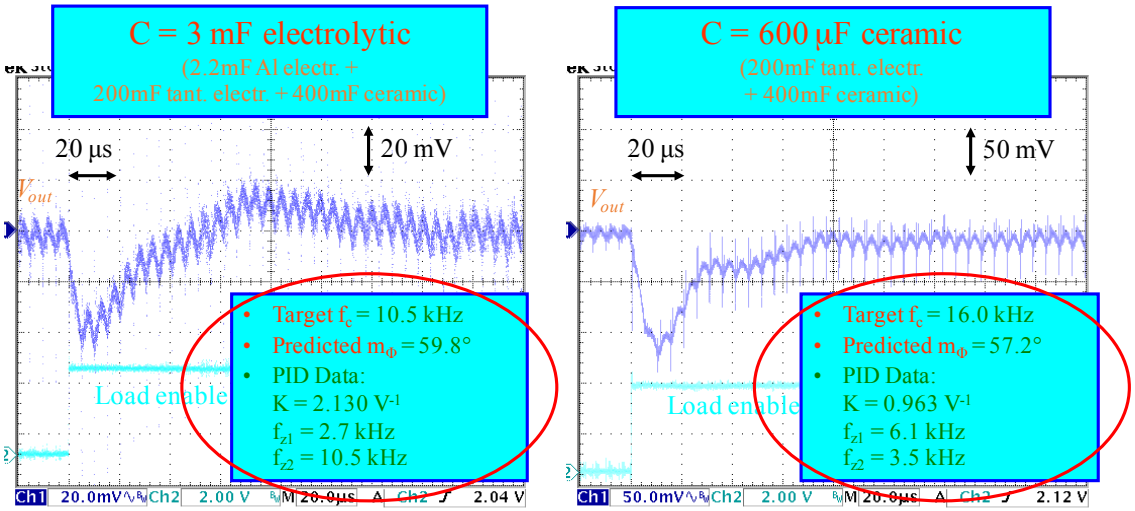
System-ID Autotuning Algorithm





Sys-ID Autotuner: experimental results

Post-Tuning 0→9A load transients with two different capacitive loads
12V-1.5V Synchronous Buck Converter,
L = 1μH, f_s=200kHz



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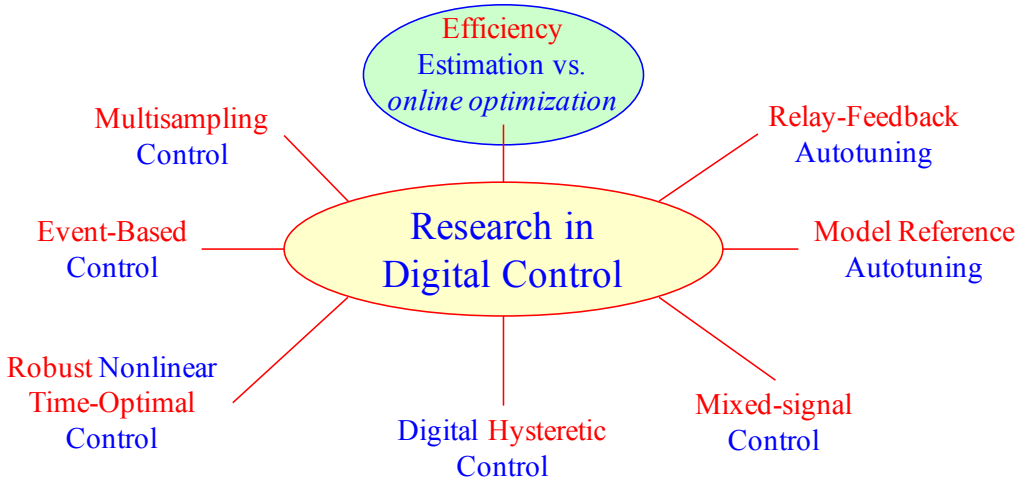
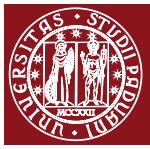
2. Offer new features, not available with analog ICs





Digital Online Efficiency Optimization of dc-dc Converters

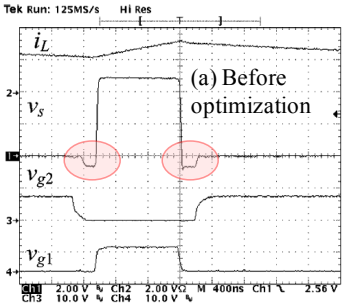
- Traditional approach to efficiency improvement:
  - "Optimization" carried out during the design phase and limited to a specific operating point or narrow operating range
  - Often topological modifications/ancillary elements are required to mitigate efficiency loss outside the optimal range
  - Fixed modulation scheme ➔ converter capabilities not fully exploited

Digital Online Efficiency Optimization of dc-dc Converters

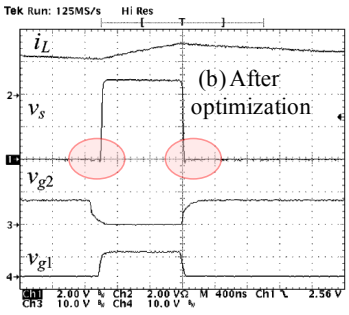
- Digital online efficiency optimization:
  - Exploit converter degrees of freedom, dynamically adjust operation to reach and track the maximum efficiency point
  - No topological modifications, transfer additional complexity to the controller rather than to the (more expensive) power stage
  - Inherently exploit maximum efficiency of a given topology and for a given operating point (e.g. mixed soft/hard switching operation)
  - Advanced control / modulation strategies facilitated by the digital approach

Digital Online Efficiency Optimization of dc-dc Converters

- Example
  - From [56]: V. Yousefsadeh and D. Maksimovic, "Sensorless optimization of dead times in dc-dc converters with synchronous rectifiers," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 994–1002, Jul. 2006
  - Sensorless dead time optimization in a synchronous buck dc-dc converter
  - Efficiency improvement from (a) 87.3 % (before optimization) to (b) 92.4 % (after optimization)

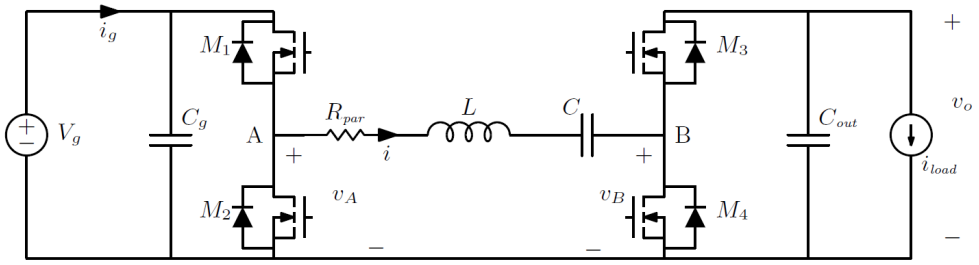


(a)



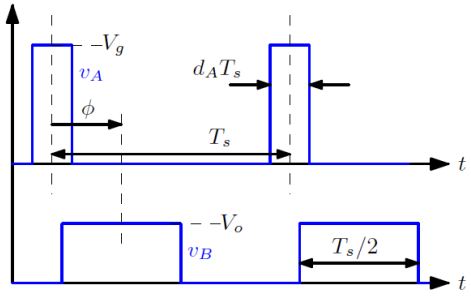
(b)

Dual Half-Bridge Series Resonant Converter

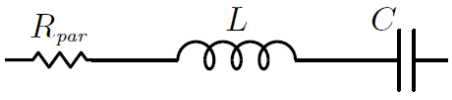


A number of degrees of freedom are offered by the DHB–SRC topology:

- Duty cycle d_A of first leg
- Duty cycle d_B of second leg
- Phase lag ϕ between control signals
- Switching frequency f_s

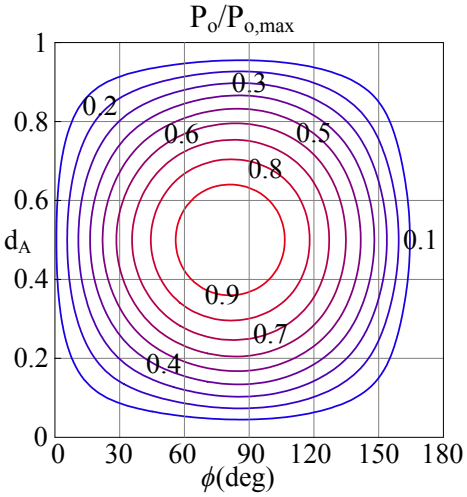


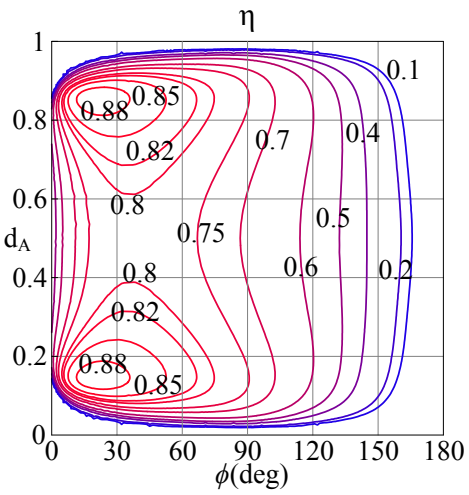
Output Power and Efficiency Contour Plots



$$R_{PAR} = ESR_L + ESR_C + 2R_{on}$$

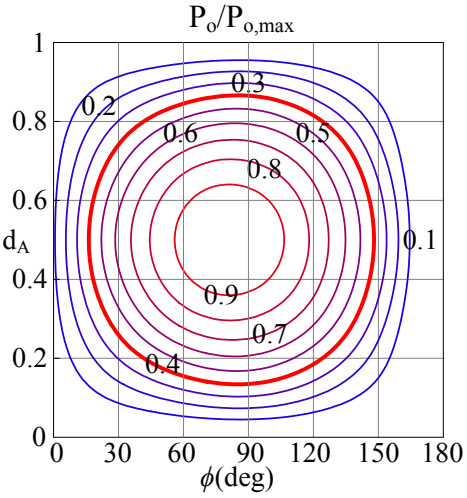
$$\begin{cases} d_B = 0.5 \\ f_s = \text{constant} \end{cases}$$

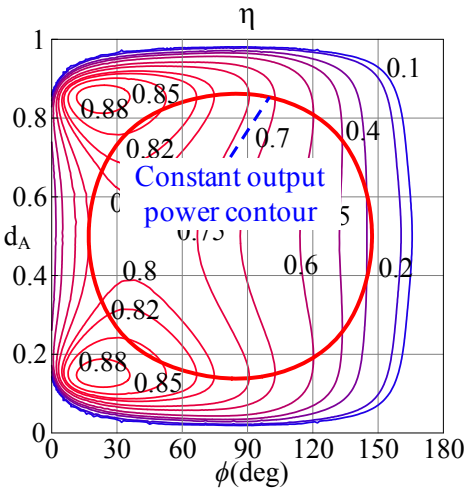




Maximum Efficiency Point

- Infinite (d_A, ϕ) configurations correspond to the *same* output power
- Among these, an optimal control input exists which maximizes efficiency





Maximum Efficiency Point

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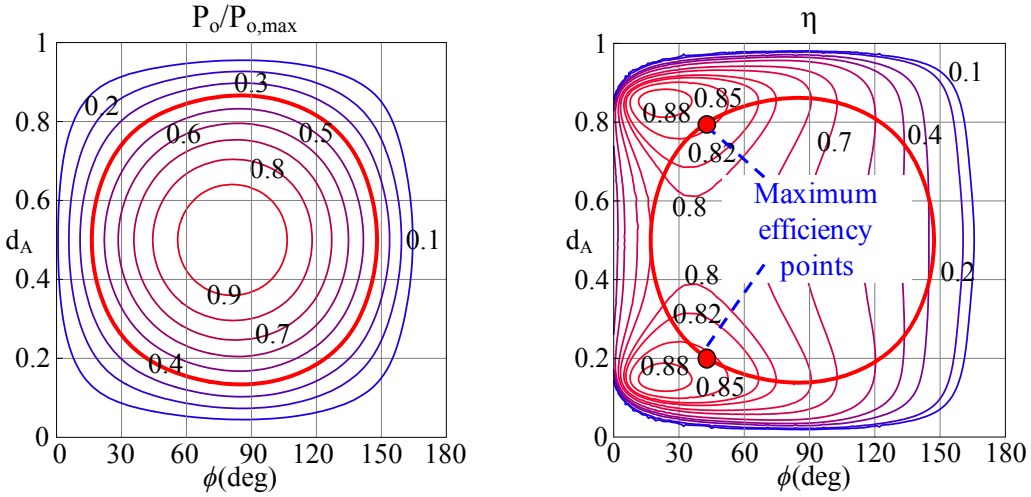
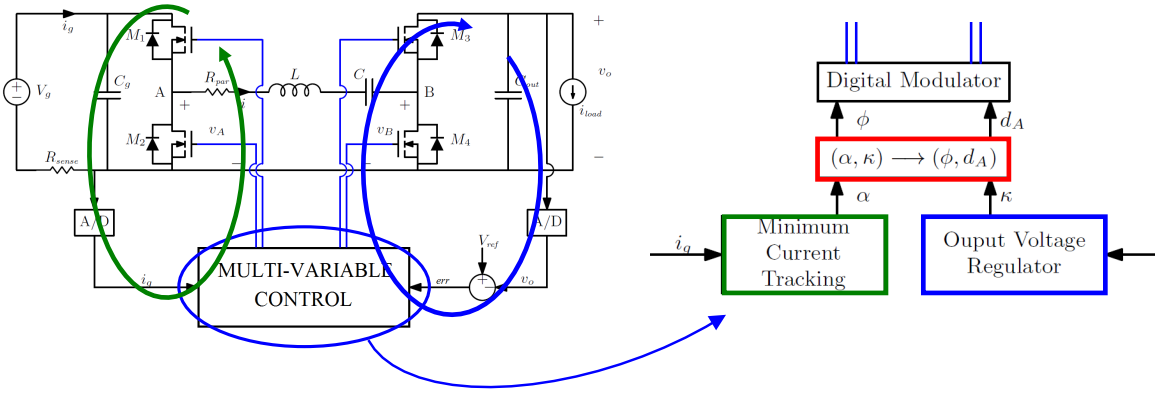


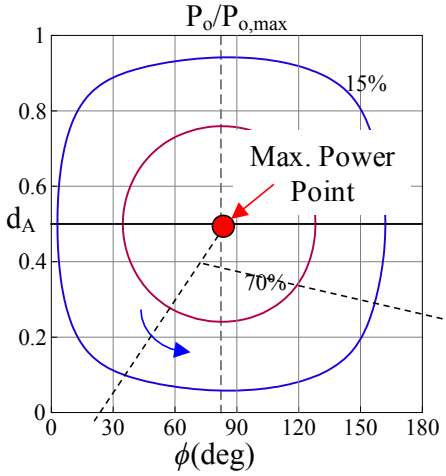
Investigated Approach for Online Efficiency Optimization



- Two loops:
  - Regulation loop (command κ) regulating the output voltage
  - Slower optimization loop (command α) minimizes the input current using a minimum current tracking algorithm (e.g. Perturb&Observe)
- Choice of the (α,κ)→(ϕ,d_A) map is crucial to the robustness of the control

Investigated Approach for Online Efficiency Optimization

Control input is constrained to lie on a straight line passing through the maximum power point:

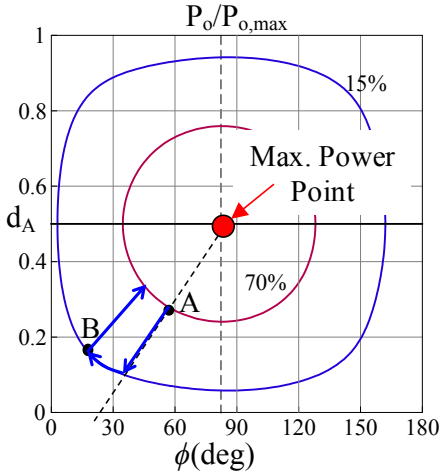


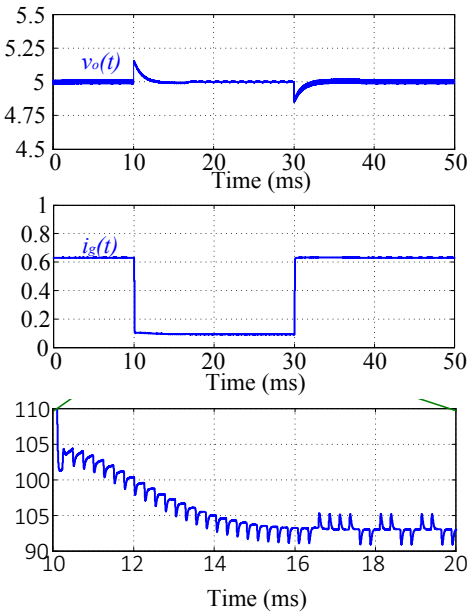
$$\begin{cases} \phi = \kappa \\ d_A = \alpha\left(\kappa - \frac{\pi}{2}\right) + 0.5 \end{cases}$$

➔ α determines the slope of the control line

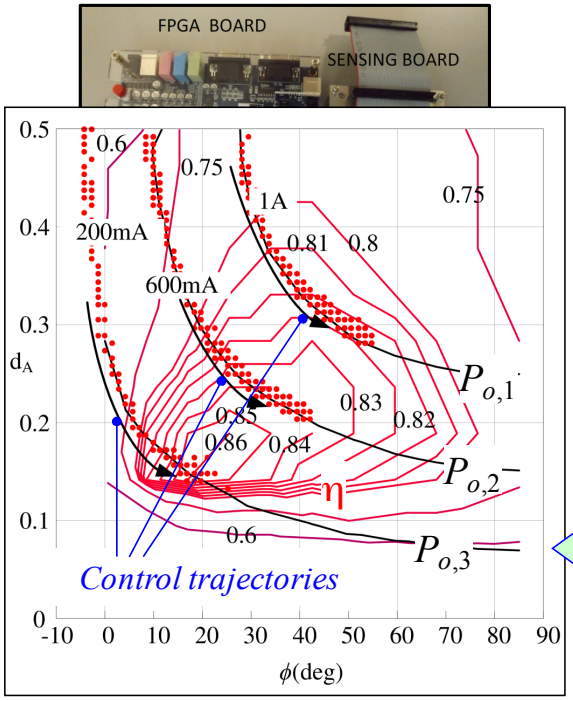
Investigated Approach for Online Efficiency Optimization

Control input is constrained to lie on a straight line passing through the maximum power point:





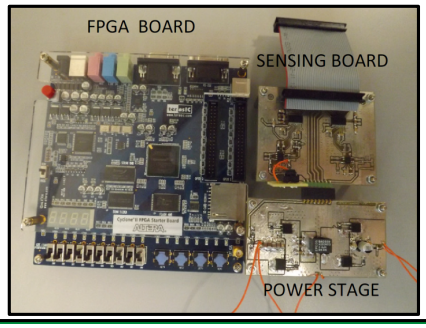
Online Efficiency Optimization: Experimental Results

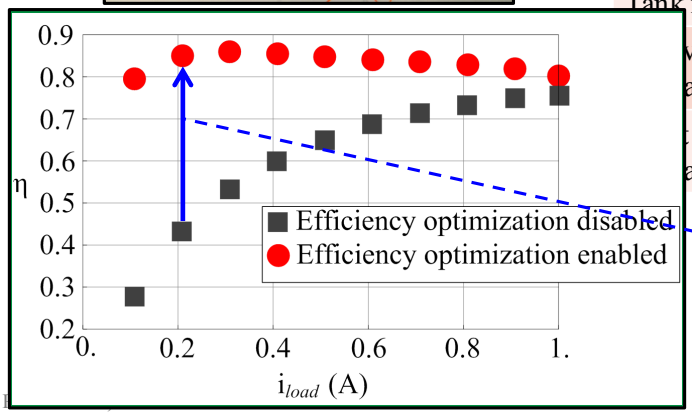


Switching frequency f_s	200 kHz
Input Voltage V_g	12 V
Output Voltage	5 V
Nominal output current	1 A
Tank capacitance	630 nF
Tank inductance	2.1 μH
Equivalent tank resistance R_{par}	0.22 Ω
Input current sensing resistance	0.2 Ω

Efficiency optimization as seen on the (d_A, ϕ) plane (experimental)

Online Efficiency Optimization: Experimental Results





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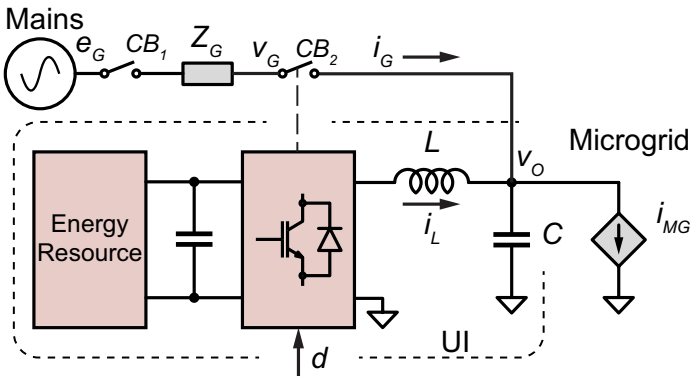
Efficiency Improvement

Part V
Oversampled Current Controller for Grid-Connected Inverters

Application example: Interfacing DERs to the Utility

- **Utility Interface**: converter interfacing distributed energy resource (DER) to the mains.



- **Grid-supporting** behaviour during **grid-tied operation**.
- **Grid-forming** behaviour during **islanded operation**.

- **High-performance current controllers** bring several advantages in utility interface converters operation, like:
  - sustaining fast load transients
  - compensating harmonic currents
  - rejecting grid disturbances

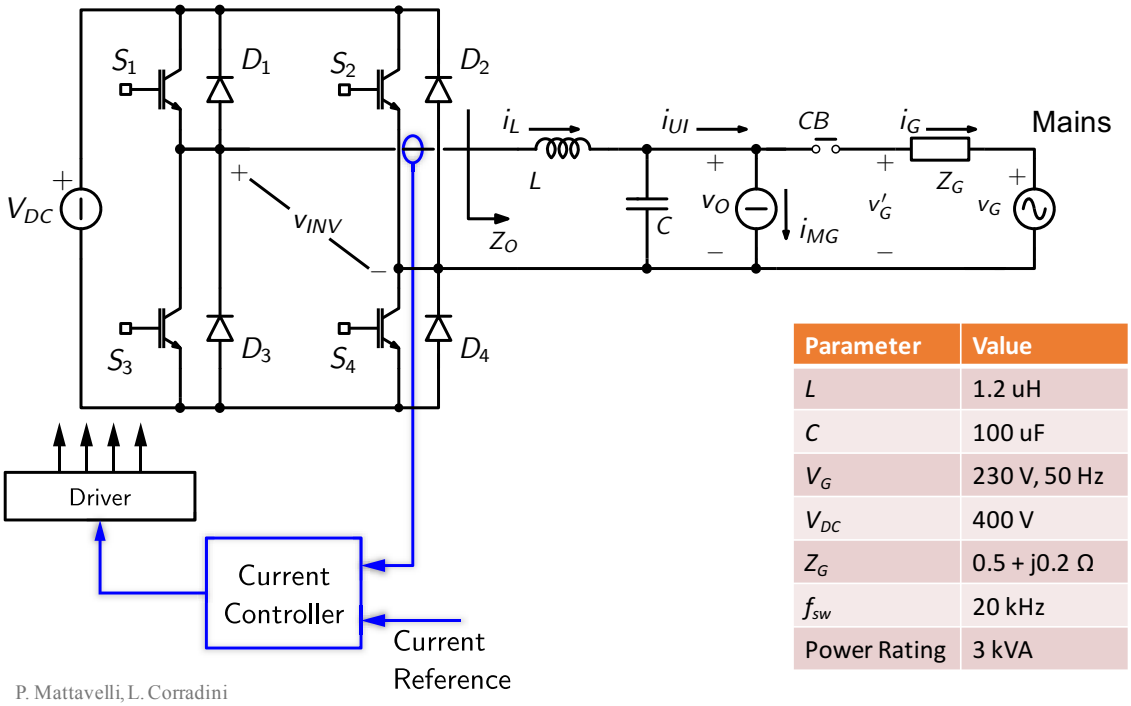
Motivations of comparing current controller in utility applications

- **Comparing** three different fully digital, oversampled, large bandwidth **inverter current controllers**:
  - **Proportional-Integral Controller**
  - **Predictive Controller**

    Buso *et al*, "Oversampled Dead-Beat Current Controller for Voltage Source Sonverters," *IEEE APEC Conf. Proc.*, March 2015.
  - **Hysteresis Controller**

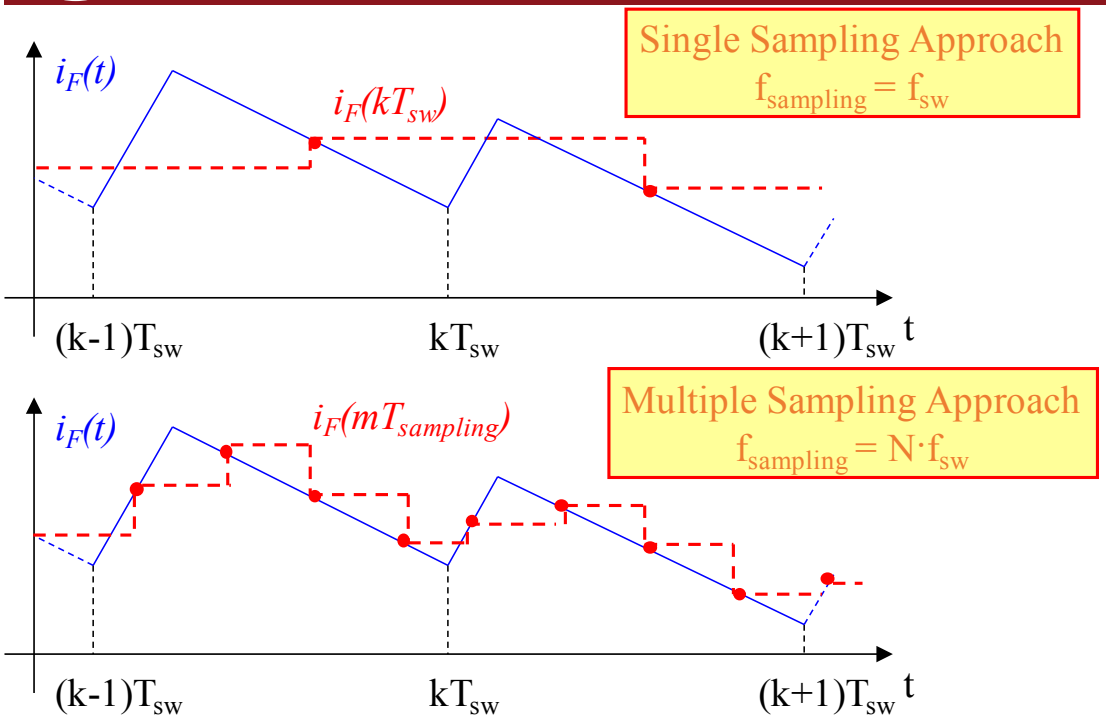
    Buso *et al*, "A Non-linear Wide Bandwidth Digital Current Controller for DC-DC and DC-AC Converters," *IEEE Trans. Ind. Electron.*, 2015.
- **Providing exprimental verification** of analytical/simulation analysis of the three controller solutions.
- Identifying which controller attains the **highest performance** when adopted as the inner current control loop in a **microgrid utility interface converter**.

Considered Topology

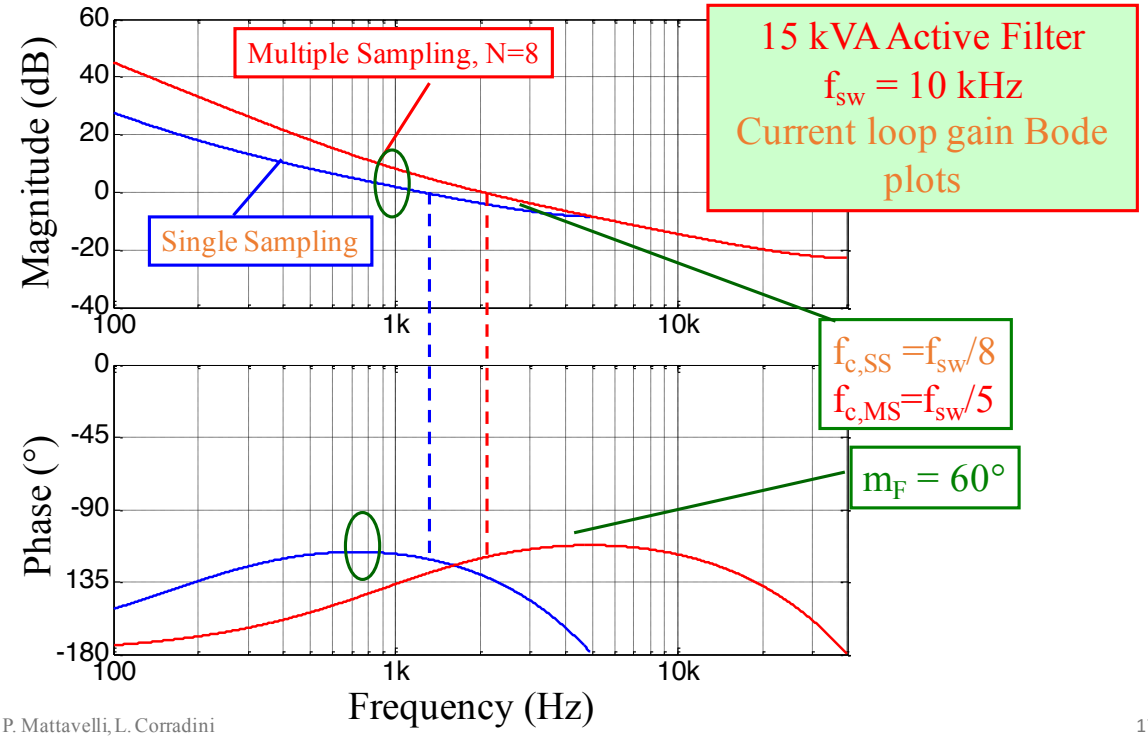


Parameter	Value
L	1.2 uH
C	100 uF
V_G	230 V, 50 Hz
V_{DC}	400 V
Z_G	0.5 + j0.2 Ω
f_{sw}	20 kHz
Power Rating	3 kVA

Sampling Approaches



Design Example: single vs multiple sampling

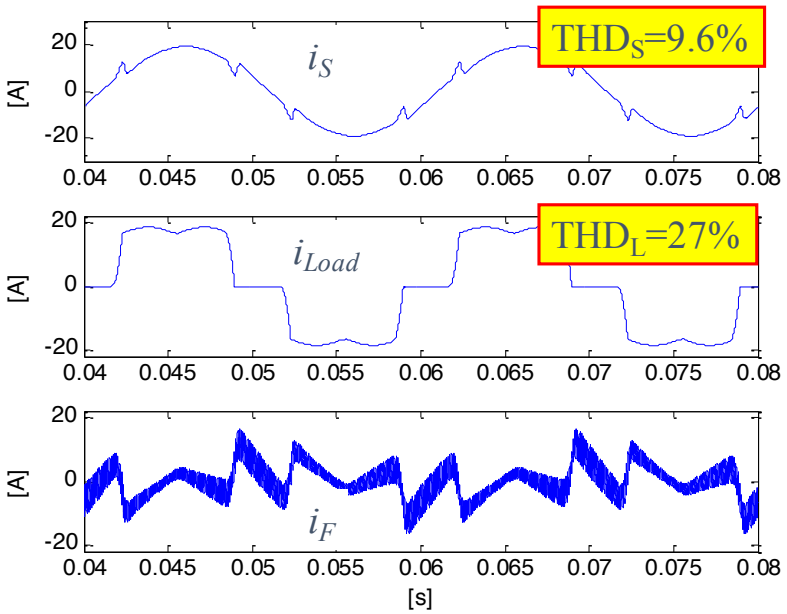


Single Sampling Current Control Simulation

15 kVA APF with three-phase diode rectifier load

f_{sw} = 10kHz

Current Control:
$f_c = f_{sw}/8$
$m_F = 60°$



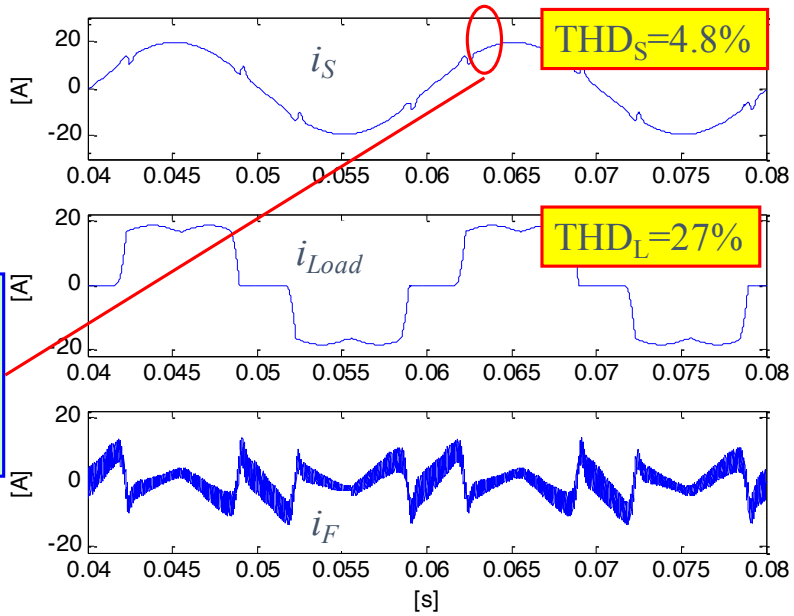
Multiple-sampling Current Control Simulation

15 kVA APF with three-phase diode rectifier load

f_{sw} = 10kHz

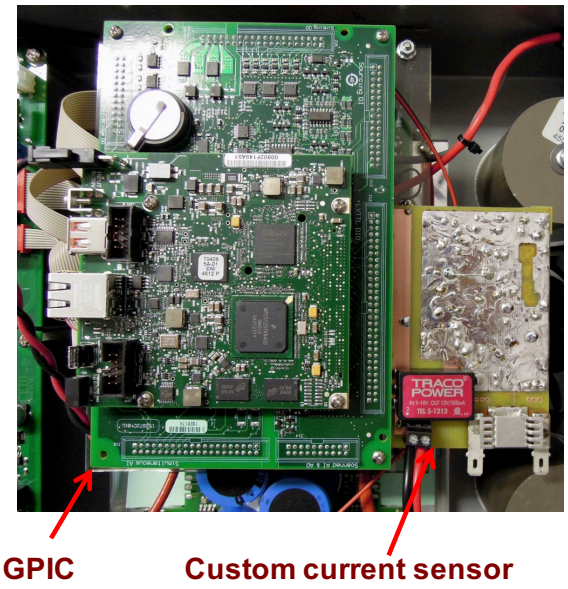
Current Control:
$f_c = f_{sw}/5$
$m_F = 60°$

Line Current THD is halved with respect to the single sampling solution

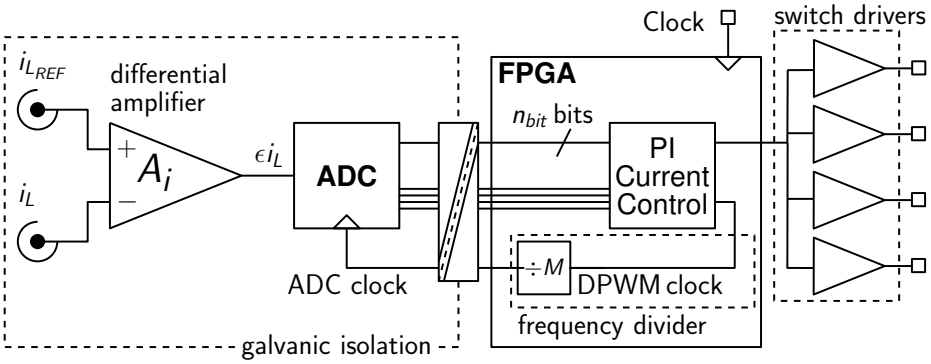


Controller Hardware

- LabVIEW environment to implement control algorithms.
- Control hardware: GPIC board.
- Custom high performance external AI as sensing device connected to the FPGA of GPIC:
  - Resolution: 12-bit
  - Analog bandwidth: 200 kHz
  - Sampling rate: 40 MSample/s
  - CMRR: 80dB



PI Current Controller



Modulator transfer function:

$$G_{PWM}(s) = k_{i,sense}\frac{2V_{DC}}{N}\cdot e^{-\frac{sT_{SW}}{2Q}}$$

Output impedance:

$$Z_O(s) = \frac{1}{sC}//Z_G(s) + sL + ESR_L \cong sL$$

PI regulator transfer function:

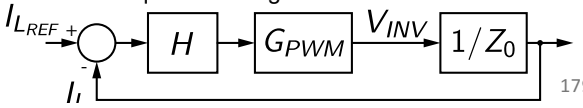
$$H(s) = K_P + \frac{K_I}{s}$$

Current Controller Transfer Function:

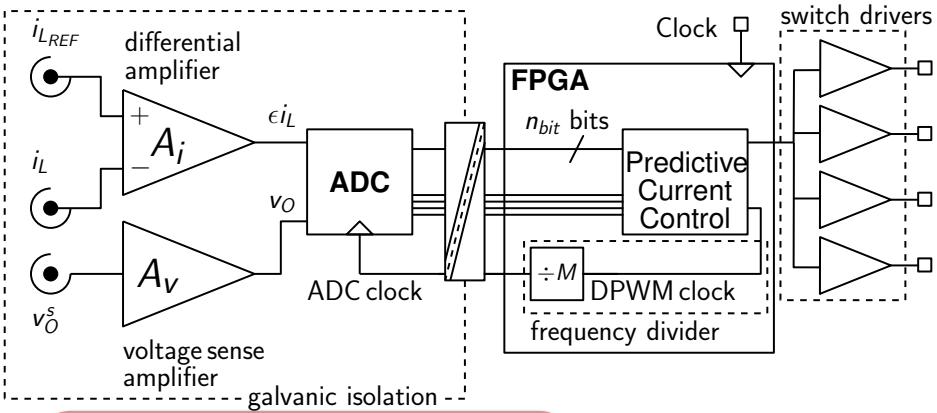
$$W_{I_{PI}}(s) = \frac{I_L(s)}{I_{L_{REF}}(s)} = \frac{\frac{G_{PWM}(s)}{Z_O(s)}H(s)}{1+\frac{G_{PWM}(s)}{Z_O(s)}H(s)}$$

crossover frequency

- Adequate to design the PI controller



Predictive Current Controller



Predictive Model:

$$v_{INV}(k) = 2V_{DC}\, L\, f_{sw}\, \epsilon i_L(k) + v_O(k)$$

Plant transfer function:

$$G(z) = \frac{i_L(z)}{v_{INV}(z)} = \frac{T_{SW}}{2L}\frac{z^{-1}}{1-z^{-1}}$$

Controller transfer function:

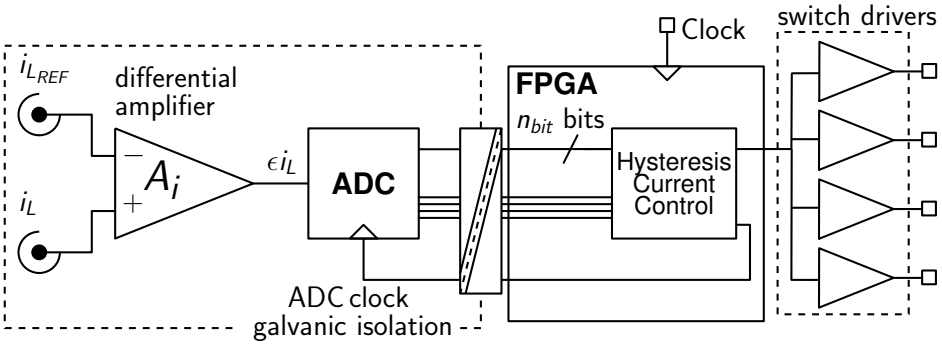
$$H(z) = \frac{v_{INV}(z)}{\epsilon i(z)} = 2Lf_{SW}$$

Current Controller Transfer Function:

$$W_{I_{DB}}(z) = \frac{I_L(z)}{I_{L_{REF}}(z)} = \frac{G(z)H(z)}{1+G(z)H(z)} = z^{-1}$$

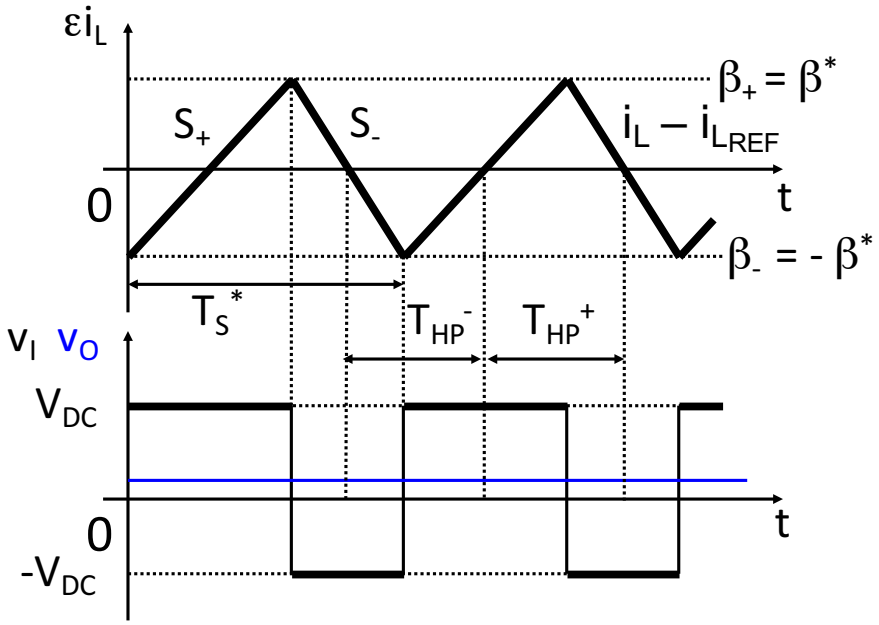
$$W_{I_{DB}}(s) = e^{-\frac{sT_{SW}}{2}}$$

Hysteresis Current Controller

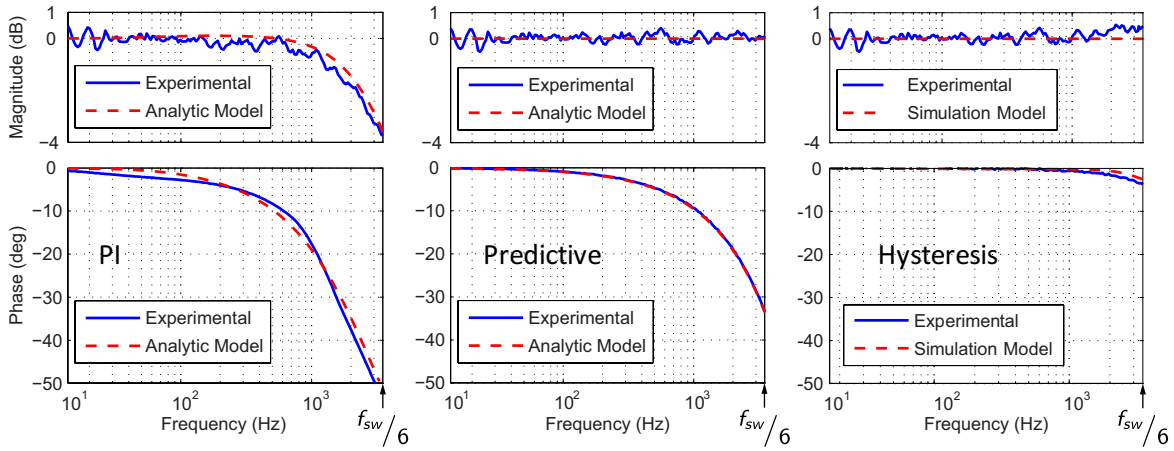


- An accurate *simulation model* was implemented that allows to test the controller response to small sinusoidal perturbations of the steady state reference current.
- Based on that, the perturbation effect can be predicted and the controller's phase lag can be *numerically* estimated.

Hysteresis Current Controller



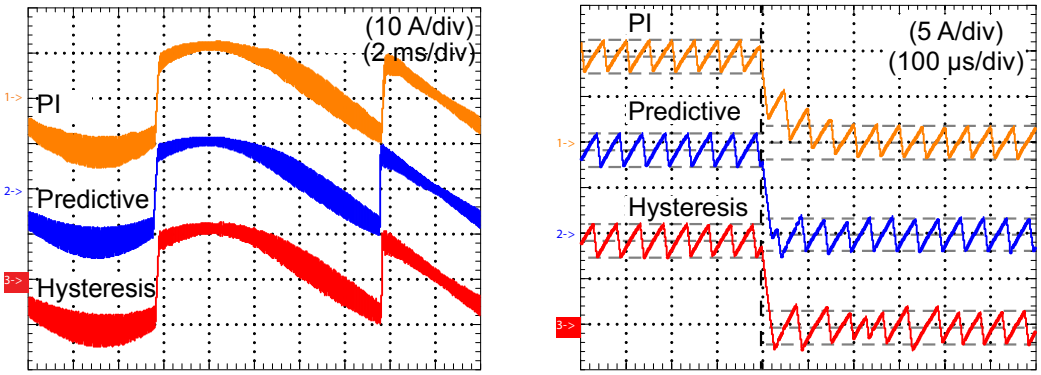
Small-Signal Performances



- Measured phase shift at **3 kHz** ($\simeq f_{sw}/6$)
  - PI controller: -49°
  - Predictive controller: -28°
  - Hysteresis controller: -3°

- Good match between experimental and analytical/simulation results.
- All the controllers guarantee a high performance level.

Large-Signal Performances



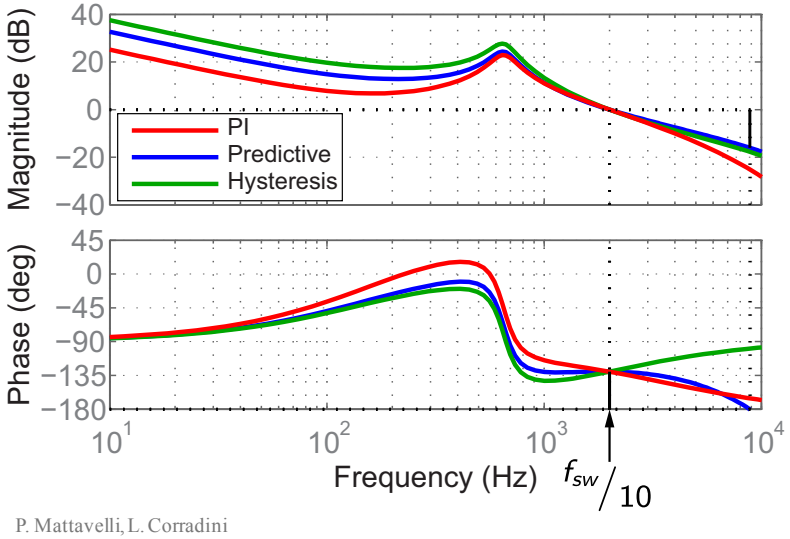
(a) **(b)**

(a) Response to 180° phase steps of a sinusoidal reference current during grid-tied operation (v_G (AC) = 230 VRMS , f = 50 Hz).

(b) Response to a negative step of the reference current (v_O (DC) = 280 V).

Utility Interface Voltage Control

- **Open-loop *voltage* gains** obtained with the considered current controllers
- **PI voltage regulator**, designed for 2 kHz crossover frequency, 50° phase margin.

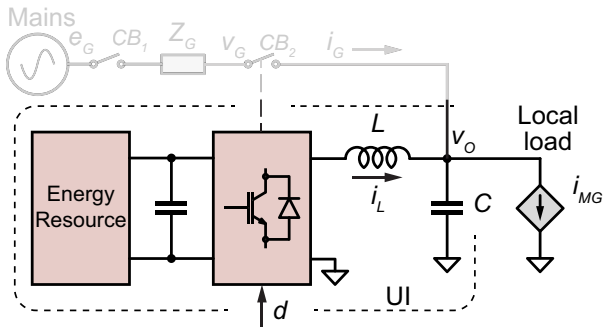


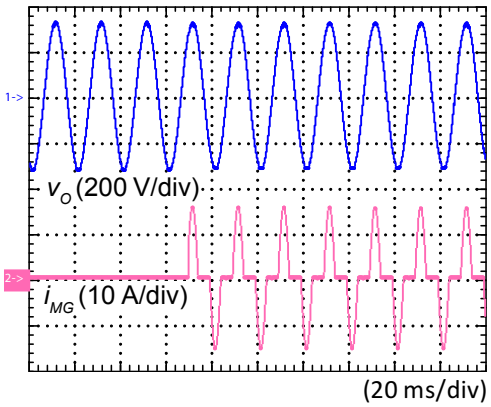
Summary of Initial Results

- All the considered controllers (oversampled PI, predictive, hysteresis) shown high performance levels.
- In the bandwidth [10 Hz, 3.0 kHz] the amplitude response is practically flat while the phase shift is minimum for the hysteresis controller (equal to -3° at 3.0 kHz) and maximum for the PI controller (equal to -49° at 3.0 kHz).
- Reference step changes are detected with both minimum delay and rise time for the hysteresis controller. A similar behaviour is shown by the predictive controller. PI regulator response is consistent with its small-signal bandwidth.
- THD performance of PI: 1.52 %; Predictive: 0.82 %; Hysteresis: 1.47 %, in traking a 10 A_{pk} sine wave (voltage THD = 3 %).

Utility Interface Results

- **Grid-forming mode** (islanded operation) with a 1.5 kW ($P_{UI}^{rated}/2$) non-linear load, crest factor CF=2.

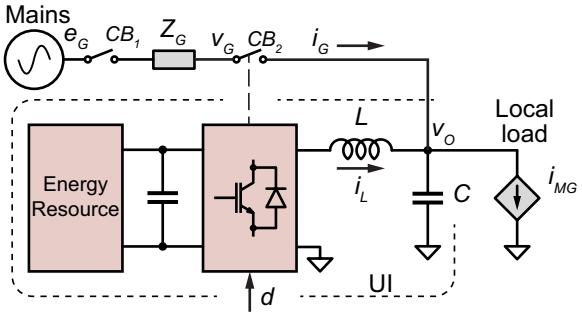




	No load	47 Ω(1)	0.5 kW(2)	1.0 kW(2)	1.5 kW(2)
THD @ PCC	0.09 %	0.16 %	0.35 %	0.72 %	1.04 %

(1) Purely resistive load.
(2) Programmable electronic load, crest factor $CF = 2$.

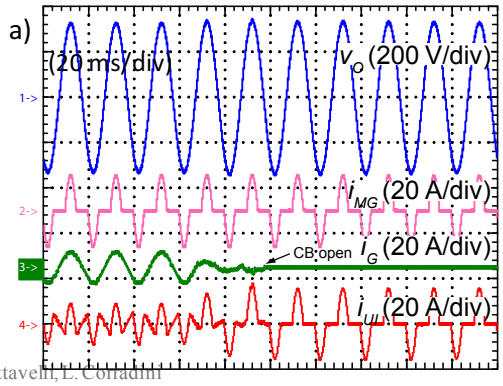
Utility Interface Results

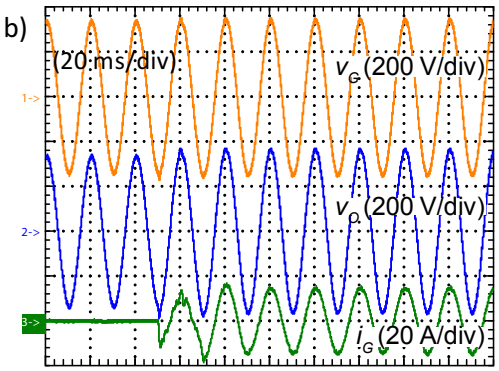


Grid-connected / Islanded operation:

a) Disconnection of UI from the manis

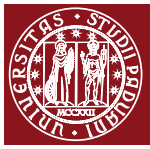
b) Connection of the UI to the mains





Tutorial Summary

- Basics of digital control in power electronics has been outlined for high-frequency dc-dc converters, including:
  - Modulation delay
  - Modeling techniques
  - Controller design
- A set of advanced applications of Digital Control has been addressed:
  - Time- optimal control
  - Autotuning
  - Efficiency optimization
- Oversampling techniques for inverters have been described



Thank you for your kind attention!

Selected References

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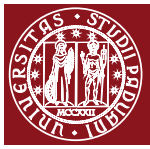

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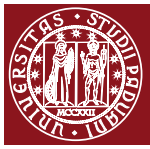

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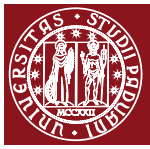

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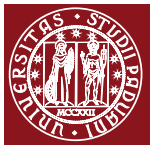

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